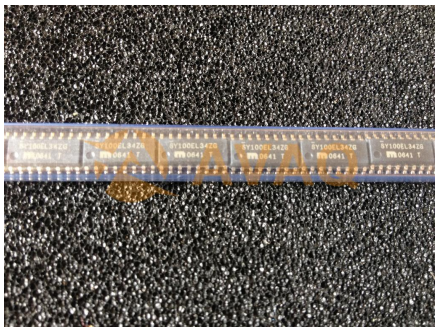
SY100EL34ZG

Clock Divider Buffer 3-OUT 1-IN 1:3 16-Pin SOIC N Tube

Manufacturer:	Microchip Technology, Inc
Package/Case:	SOP16
Product Type:	Drivers
RoHS:	RoHS Compliant/Lead free
Lifecycle:	Active



Images are for reference only

Inquiry

General Description

The SY10/100EL34/L are low skew ÷2, ÷4, ÷8 clock generation chips designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The devices can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. In addition, by using the VBB output, a sinusoidal source can be ACcoupled into the device. If a single-ended input is to be used, the VBB output should be connected to the CLK input and bypassed to ground via a 0.01µF capacitor.The VBB output is designed to act as the switching reference for the input of the EL34/L under single-ended input conditions. As a result, this pin can only source/ sink up to 0.5mA of current.The common enable (EN) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.Upon start-up, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as for multiple EL34/Ls in a system.

Key Features

3.3V and 5V power supply options

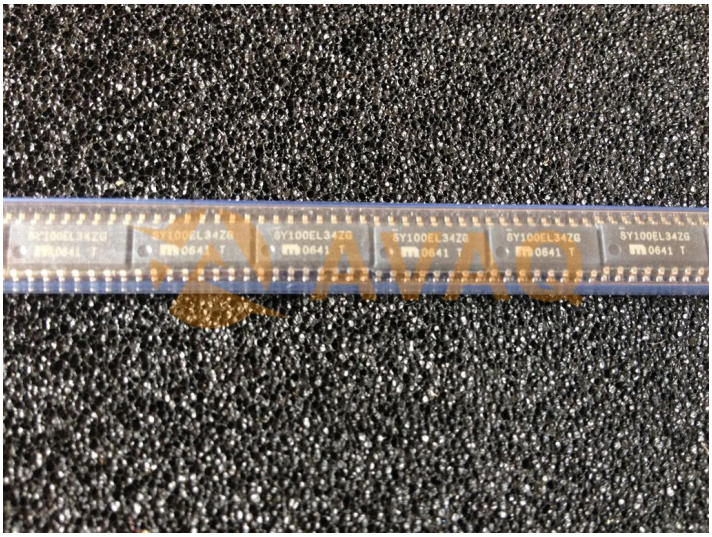
50ps output-to-output skew

Synchronous enable/disable

Master Reset for synchronization

Internal 75KΩ input pull-down resistors

Available in 16-pin SOIC package



Recommended For You

SY87729LHY

Microchip Technology, Inc

QFP32

SY87701ALHG

Microchip Technology, Inc

TQFP32

SY89296UMG

Microchip Technology, Inc

VQFN

SY89297UMG

Microchip Technology, Inc

QFN24

SY89295UMG

Microchip Technology, Inc

QFN

SY89874UMG

Microchip Technology, Inc

QFN

SY87700ALHG

Microchip Technology, Inc

QFP32

SY87739LHY

Microchip Technology, Inc

TQFP32

SY89202UMG

Microchip Technology, Inc

QFN

SY89876LMG

Microchip Technology, Inc

QFN

SY100EP196VTG

Microchip Technology, Inc

TQFP32

SY89831UMG

Microchip Technology, Inc

QFN

SY89833ALMG

Microchip Technology, Inc

16-VFQFN

SY89297UMH

Microchip Technology, Inc

VQFN

SY87721LHG

Microchip Technology, Inc

64-TQFP