ANALOG DEVICES

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APPLICATION NOTE

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Using the AD834 in DC to 500 MHz Applications: RMS-to-DC Conversion, Voltage-Controlled Amplifiers, and Video Switches

by Mark Elbert and Barrie Gilbert

INTRODUCTION

The AD834 is the fastest four quadrant multiplier available, having a useful bandwidth of 800 MHz, compared to the 60 MHz bandwidth of the AD539 two-quadrant multiplier, the 10 MHz bandwidth of the AD734 four-quadrant multiplier, or the 1 MHz bandwidth of the industry-standard AD534 four-quadrant multiplier. Its monolithic construction and high speed makes the AD834 a candidate for such HF applications as balanced modulation-demodulation, power measurement, gain control, and video switching, at frequencies that were previously beyond the scope of analog multipliers.

The AD834 does not sacrifice accuracy to achieve its speed. In common with all of the Analog Devices multipliers, laser trimming is used during manufacture to null input and output offsets and to establish precise scaling. In typical applications the total static error can be held to less than ±0.5%.

It is available in 8-pin plastic DIP, SOIC, and ceramic packages for the commercial, industrial, and military temperature ranges and operates from ±5 V supplies.

The main challenge in using the AD834 arises from its current-mode output stage. In order to maintain the highest possible bandwidth, the AD834's outputs are in the form of a pair of differential currents from open collectors. This is an inconvenience when a more conventional ground-referenced voltage output is needed. Thus, this application note discusses methods for the accurate conversion of these currents to a single-sided ground-referenced voltage.

These applications include a wideband mean-square detector, an rms-to-dc converter, two wideband voltage-controlled amplifiers, a high-speed video switch, and transformer-coupled output circuits. These applications provide the user with a complete and proven solution, in many cases including recommended sources for critical components.

OVERVIEW OF THE AD834

The AD834, shown in block schematic form in Figure 1, is the outcome of Analog Devices' continuing dedication to high-accuracy analog signal processing. In particular,

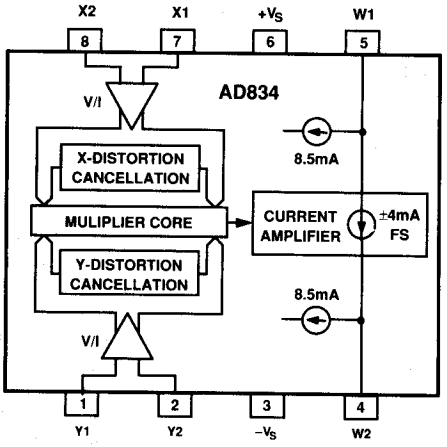


Figure 1. AD834 Block Diagram

it incorporates the experience gained in twenty years of manufacturing analog multipliers. The part is constructed on a 3 GHz epitaxial bipolar transistor process using laser-trimmed thin-film resistors. Attention to many subtle details has resulted in unusually low distortion and noise. Figure 2 shows a more detailed, but still simplified, circuit schematic.

The X- and Y-inputs are applied to high-speed voltage-to-current (V/I) converters, having a transresistance of 285 Ω and a small-signal input resistance of about 25 kΩ. The full-scale input voltage is ±1 V for both inputs. The input bias currents are typically 45 μA. Therefore, the dc resistance seen by both inputs of a differential pair must be equal to minimize offset voltages, just as for an op amp. Resistors at the inputs also minimize the risk of

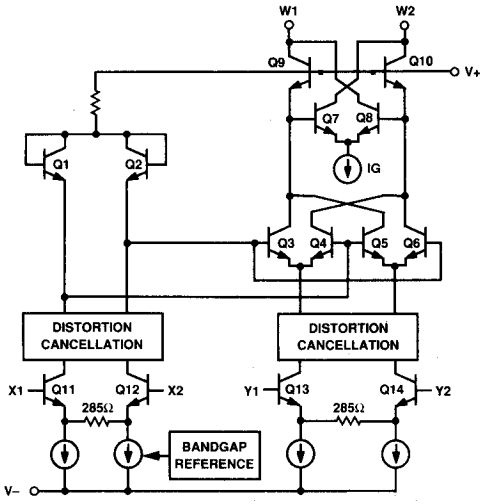


Figure 2. Simplified AD834 Schematic

high frequency oscillations. The V/I converters have a common-mode range of ±1.2 V, using the recommended supply voltages. Within that range, the differential inputs exhibit a common-mode rejection of 70 dB, conservatively specified for f < 100 kHz. Even-order distortion in the V/I converters is inherently low, while distortion cancellation circuitry is included to reduce odd order nonlinearity to typically ±0.05%.

The *multiplier core* is a well-known translinear circuit. The translinear principle [Ref. 1] exploits the precise logarithmic relationship between the base-emitter voltage (V_{BE}) and collector current (I_C) of a bipolar transistor. The input and output signals of translinear circuits are always in current form. Voltage swings at the internal nodes are very small, so that parasitic junction capacitances do not have to be charged and discharged, a common cause for bandwidth reduction and slew-rate limiting. Thus, translinear multiplier cells are inherently fast; they are also readily implemented in monolithic form. However, they can introduce distortion if not carefully designed.

This distortion is due primarily to emitter area mismatches and ohmic resistances in the core transistors (Ref. 2). Using the traditional convention in naming the channels, as shown in Figure 2, the X channel is susceptible to these effects, while the Y signal-path is essentially linear (the four output devices, Q3 through Q6, behaving in many respects like common-base stages, or cascodes). Therefore, the signal requiring the lowest possible distortion should always be handled by the Y channel. For example, in a balanced modulator application, the carrier (local oscillator voltage) should be applied to the X input and the baseband signal to the Y input.

The output from the core is in the form of a pair of differential currents. Now, the scaling of these currents is customarily controlled by adjustment of the bias currents in the V/I converter used on the X-input, which also determines the currents in the diode-connected transistors, Q1 and Q2.

In classical voltage-output multipliers, the range of adjustment needed to absorb the inevitable resistor mismatches is small, and this method of trimming the scaling factor is acceptable. In the AD834, however, the transfer function involves the two input voltages V_X and V_Y, the scaling voltage (generated in the band-gap reference circuit, and trimmed to an accurate value which is assumed here to be 1 V) and the output current, I_W:

$$I_W = \frac{V_X V_Y}{1V} \cdot \frac{I}{R} \qquad (1)$$

In this expression, the value of a resistance, R, determines the calibration of the output current. As fabricated, thin-film resistors have an initial uncertainty which can be as large as ±20%, and the customary methods of trimming the scale factor would result in other compromises (for example, erosion of the available signal range in the X-input V/I converter).

Therefore, the AD834 uses a "Gilbert gain-cell" [Reference 3] after the core to provide the needed adjustment of the effective value of R, which, in fact, is achieved by varying the current gain of this cell through trimming the current I_G. R, after the I_G trim, has an effective value of 250 Ω, resulting in a full-scale output current of ±4 mA when both inputs are at their full-scale value of ±1 V. The typical current-gain is 1.6, and because this type of amplifier is very fast and buffers the core outputs, the overall bandwidth of the multiplier is actually enhanced over that which would be obtained using the core outputs directly.

The bias currents from the core, and the gain-setting current I_G, result in a fairly large standing current—typically 8.5 mA—which flows into the outputs W1 and W2 (Pins 4 and 5). Only the *differential* output is precisely specified to be ±4 mA.

The output currents can be converted back to voltages in a variety of ways. In the simplest case, load resistors connected to the positive supply might be used, but these do not convert the (two) differential outputs to a single-sided voltage.

For the AD834 to operate properly, the output Pins (4 and 5) must be pulled above V+ to avoid saturation of Q7–Q10. To avoid using a separate supply to do this, several of the circuits included here use a voltage-dropping resistor in series with the positive supply Pin (6) of the AD834; this is a higher value than necessary for decoupling purposes.

This dropping resistor lowers the voltage at Pin 6 to provide an extra margin of bias for the output transistors. For example, in the mean-square circuit in Figure 3, 11 mA of quiescent current across the 169 Ω dropping resistor creates 1.86 V of headroom. The decoupling re-

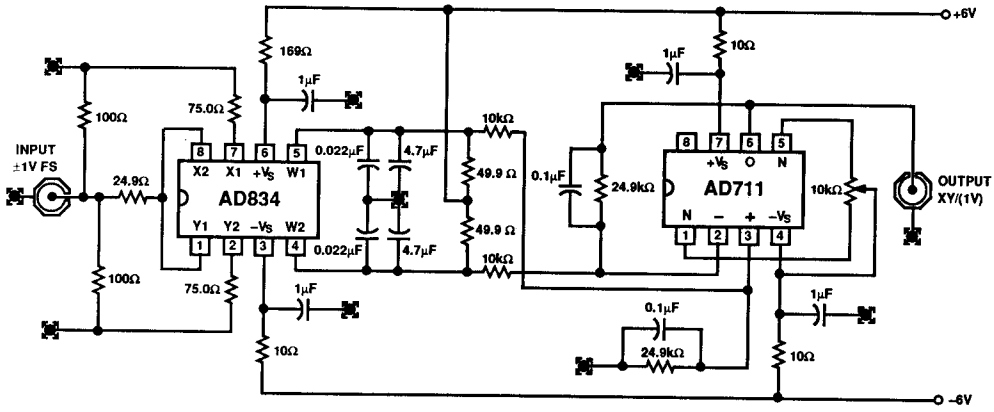


Figure 3. A DC to 500 MHz Mean Square Circuit

sistor in series with the negative supply to Pin 3 is only 10 Ω, since it is included just to decouple the supplies.

Much of this application note, however, is concerned with *more effective ways* of loading the outputs. For example, because they are fully calibrated, the outputs of two or more AD834's can be accurately summed by simply connecting them in parallel, as is done in the rms application discussed later in this application note.

MEAN-SQUARED DETECTOR

We will begin with a discussion of a mean square detector (Figure 3), whose output is a dc voltage proportional to the input power. This circuit is useful in that it requires only a calibrated signal generator and a dc voltmeter to demonstrate the very high speed of the AD834.

The input signal is applied to the X- and Y-inputs connected in parallel. The *instantaneous* output current is thus proportional to the square of the input voltage. The square of a sinusoidal input voltage of amplitude A is an offset cosine at twice the frequency:

$$A\,(sin\omega t)^2 = A^2\,(1 - cos\,2\,\omega t)/2 \qquad (2)$$

If the input to the AD834 has this sinusoidal form, then the instantaneous output current (using Equation 1) is simply

$$I_W = 2A^2\,(1 - cos2\omega t)\ mA \qquad (3)$$

the average value of which is just 2 mA for the maximum 1 V amplitude sinusoid.

The full-scale differential voltage which would be measured across Pins 4 and 5 of the AD834 is, therefore, 2 mA × (50 Ω + 50 Ω), or 200 mV. This average is extracted by the low-pass filter formed by the 4.7 μF 0.022 μF (AVX part #SR505E475MMAA and #SR505a223JAA) capacitors in conjunction with the 50 Ω collector load resistors, having a −3 dB frequency of about 650 Hz.

Two capacitors are used in parallel since the 4.7 μF capacitor uses the compact but lossy Z5U dielectric material while the 22 μF capacitor uses a high Q NPO dielectric which ensures good filtering at the highest frequencies. Note that the 4.7 μF capacitors have a −20% to +80% tolerance, so their −3 dB frequency is not accurate, nor does it usually need to be. Further filtering is performed by the capacitors in shunt with the feedback resistors of the AD711 operational amplifier, configured to have a −3 dB frequency of 65 Hz.

Due to finite averaging of the circuit, there will be some ripple for low frequency inputs. For the circuit shown, a 1 kHz input will produce the mean-square plus a −42 dB 2 kHz ripple; for 100 kHz input, the ripple will be only −80 dB. Since the output is band limited, we can use a generic low speed op amp with ample common-mode range, obviating the need for level shifting. The differential gain of the amplifier can be chosen to provide a convenient scale factor.

The full-scale gain of the circuit in Figure 3 is calculated as follows. The average output current is ±2 mA for 1 V (peak) sinusoidal input, which creates ±100 mV across each 50 Ω output load resistor or 200 mV differential. The amplifier is configured for a differential gain of 2.5 (feedback resistance over source resistance), yielding a circuit gain of 0.5 V dc output for 1 V rms input.

The bandwidth of this circuit is limited by package capacitance and inductance. In the 8-pin cerdip, the multiplier's response normally starts to rise at 500 MHz due to package resonance and peaks at 800 MHz before rolling off. A 24.9 Ω resistor at the input dampens the resonance yielding an essentially flat response out to 800 MHz. (The package inductance will be different for a surface mount AD834.) Figure 4 shows the results over frequency for three different power levels using the test configuration shown in Figure 5.

Neglecting the 24.9 Ω in series with the high impedance inputs, the input resistance to the mean square circuit in Figure 3 is 50 Ω. Since the full-scale input range is ±1 V, the maximum measurable power with a 50 Ω input load is 10 mW (20 dBm), assuming a sinusoidal input.

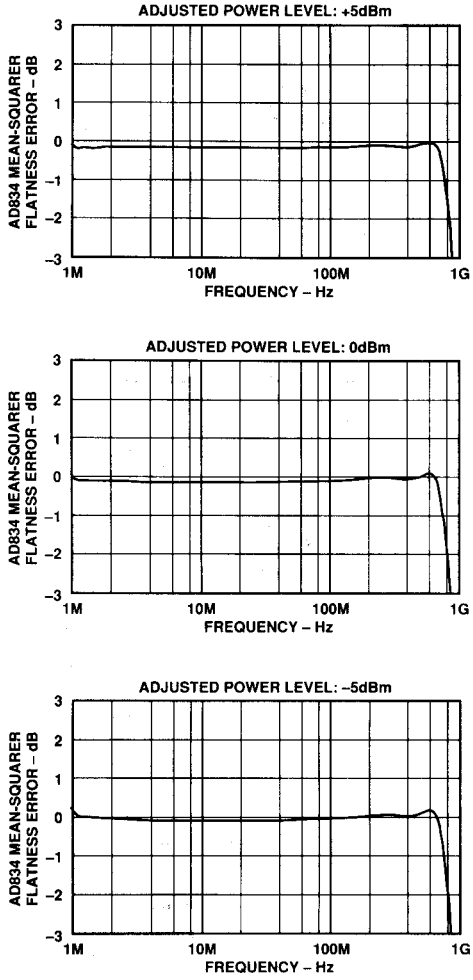


Figure 4. Frequency Response of Mean Square Circuit for Input Power Levels of −5 dBm, 0 dBm, and +5 dBm

For greater input ranges, a voltage divider with a series resistance of 50 Ω at the input will scale down the voltage seen by the AD834 while maintaining a proper termination resistance. For example, if the input signal is applied to a 45 Ω resistor in series with a 5 Ω resistor to ground, then taking the AD834's input from the middle node of the voltage divider provides 20 dB attenuation of the input signal, while maintaining a termination resistance of 50 Ω (45 Ω + 5 Ω).

Detection of low power signals is limited by dc offsets and the common-mode rejection of the op amp. For example, a −20 dBm signal, corresponding to 22.4 mV rms across 50 Ω, would result in a 4.5% error in the presence of only 1 mV of offset in the op amp. A 10% error can occur if the AD834's X channel offset is just 2 mV.

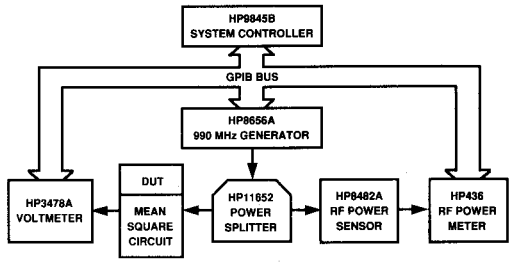


Figure 5. Test Configuration

RMS-TO-DC CONVERTER

The root mean square (rms) circuit (Figure 6) is little more than the mean square detector circuit described above followed by a square root circuit. The frequency response is determined by the front end squarer and output filter. From the mean-square discussion, the squarer functions well past 500 MHz, while the lower −3 dB frequency response is 340 Hz (100 Ω and 4.7 μF). Note that a resistor divider network at the input determines the full-scale input voltage to be ±2 V peak.

The square root function is performed by a squaring AD834 in the feedback loop of an AD711 operational amplifier. The 2N3904 transistor functions as a buffer. The resistive divider network (two 100 Ω) between the buffered output and the X and Y channel inputs of the AD834 used in the square root section determines the output scaling to be ±2 V full scale.

The outputs of the two AD834s are current-differenced. Accurate output differencing and summing is possible owing to the precision of the laser trimmed AD834 output signal current scaling. The AD711 forces the difference between the two AD834 signal current to zero. Any error in the nulling generates a voltage across the two 100 Ω pull-up resistors.

After additional filtering and level shifting by the 15 kΩ, 85 kΩ, and 0.1 μF network, the residual error is amplified by the full AD711 open loop gain. The amplified error signal forces the AD834 in the feedback loop to match its output to the mean-squaring AD834's output. The error is nulled when the rms circuit's output is equal to the square-root of the circuit's input mean-squared, hence the rms function.

The accuracy of the circuit at small signal levels is limited by inevitable offset voltages. While a nominal 0 V input with a 1 mV error to a mean-square function generates a 1 μV output error, the same input error generates a 31.6 mV output error through a square root circuit.

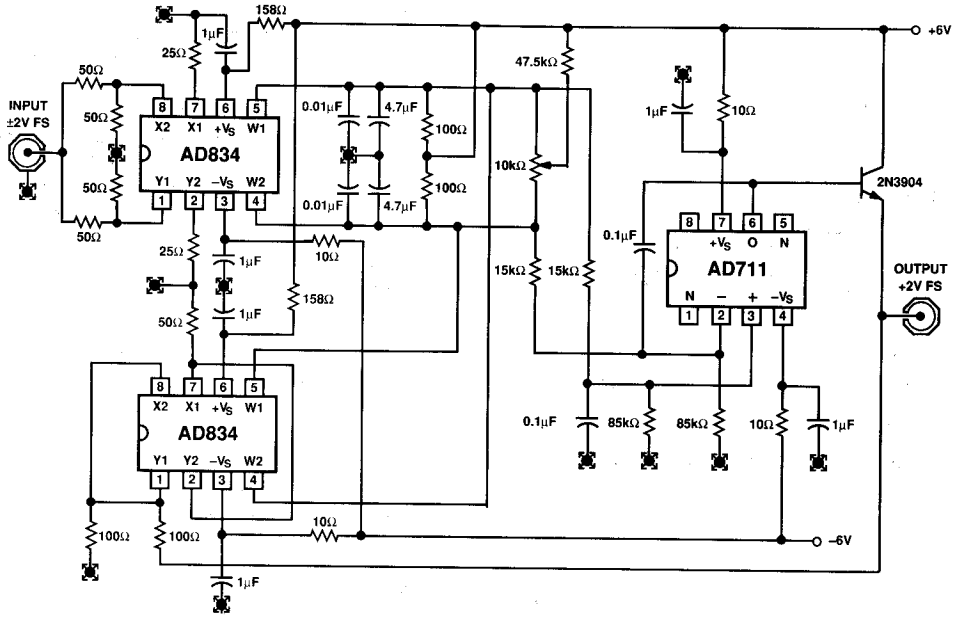


Figure 6. DC to 500 MHz RMS-to-DC Converter

DC COUPLED VCA APPLICATIONS

Where the dc response of the AD834 cannot be discarded, some form of level shifting, either passive or active must be employed, since high speed op amps often have inadequate common-mode range. The following applications show the use of active and passive level shifting circuits in the implementation of wideband voltage-controlled amplifiers.

A DC TO 60 MHz VOLTAGE-CONTROLLED AMPLIFIER USING PASSIVE LEVEL SHIFTING

Figure 7 shows the schematic of a circuit employing a passive network as a level shifter. The op amp chosen here is the AD5539.

The AD5539 is built on the same process as the AD834 and provides a 2 GHz gain-bandwidth product at high closed-loop gain. Unlike most op amps, the AD5539

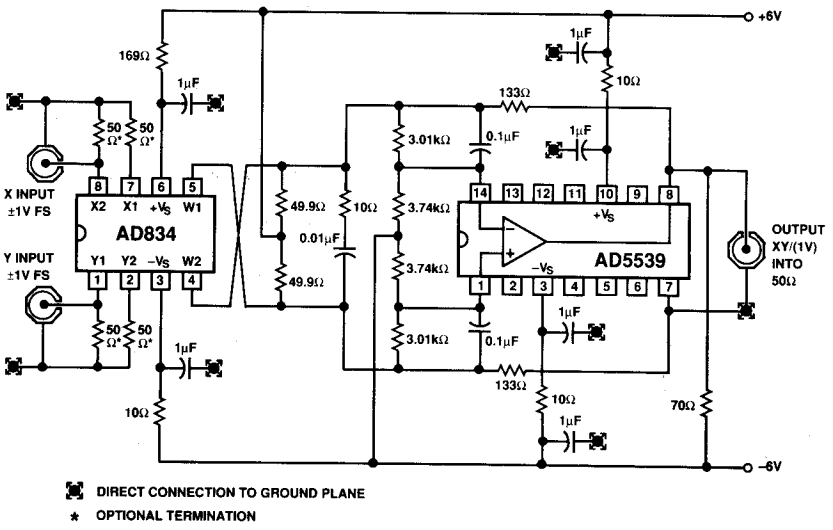


Figure 7. DC to 60 MHz Voltage-Controlled Amplifier Using Passive Level Shifting

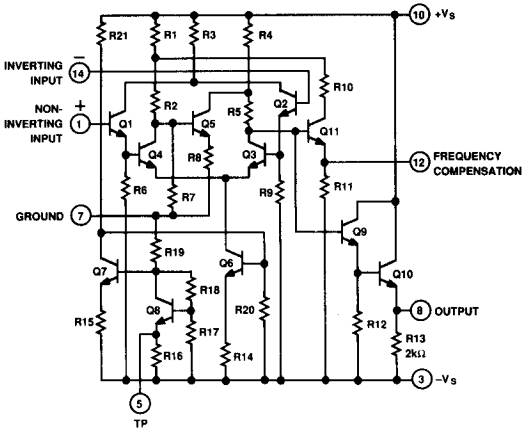


Figure 8. AD5539 Operational Amplifier Simplified Schematic

features a ground pin and an all-NPN output stage which operates in "Class A" to achieve the part's high speed (see Figure 8). Closer examination shows that there is a limited amount of "headroom" between the output node and the inputs, and between these voltages and ground. This, its high speed, and other unusual attributes of the AD5539 require special care in its use.

First, consider the consequences of its Class A output stage. In most op amps, the output can both "pull up" and "pull down" on the load, but the NPN emitter-follower output stage can only pull up. The AD5539 has an internal pull-down resistor (R11) of 2 kΩ, which can only supply two or three milliamps. A general-purpose high-speed multiplier must be able to swing to at least ±1 V while driving the minimum likely load resistance of 50 Ω. At this output level, the load current will be ±20 mA, which must therefore be supplied by an external pull-down resistor. In fact, the pull-down current must be considerably more than this, and requires careful consideration.

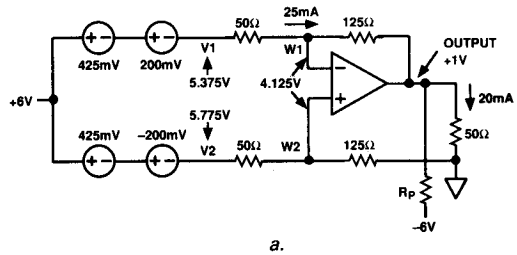
Figure 9 shows how the calculation is done. The 425 mV voltage sources are just "I_BR_C," that is, the standing current of 8.5 mA at the AD834 multiplied by the load resistor R_C, which we have here set to 50 Ω. The 200 mV sources in Figure 9 (a) are the "I_WR_C" generators when the full-scale output current is +4 mA. From here, we calculate V1 = 5.375 V and V2 = 5.775 V.

Next, we calculate the voltage at W2. Because the input current to an ideal op amp is zero, there is no loading at W2 and the voltage is simply V2 multiplied by the attenuation ratio 125/(125 + 50), or 4.125 V. Because the input voltage to an ideal op amp is zero, W1 is at the same voltage, so we can now calculate the current in the upper 50 Ω resistor as (5.375–4.125)/50 mA or 25 mA. Again, there is essentially no current at the input of the op amp, so the 25 mA all flows in the feedback resistor of 125 Ω, resulting in a voltage drop across it of 3.125 V. Finally, we calculate the output as the voltage at W1 (4.125 V) minus this drop; that is, the output is at +1 V.

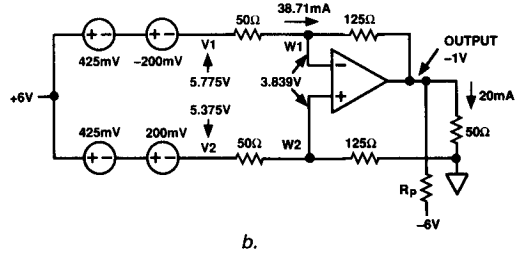
Notice a somewhat surprising result at this point: although a current of 20 mA flows into the load, a larger current, 25 mA, flows in the feedback resistor! This unusual state of affairs is due to the very low value of the feedback resistor needed to reduce the scaling factor to the desired value, and the relatively large voltage needed at the output of the AD834 to ensure proper biasing of its outputs W1 and W2. Thus, even though the load needs to be sourced 20 mA, we still need to provide at least 5 mA in the pull-down resistor R_P to bias the output emitter-follower in the AD5539. The situation gets more severe when the output current of the AD834 is reversed, because we now need to sink 20 mA in the 50 Ω load and the voltage across the feedback resistor is now even higher.

This situation is shown in Figure 9(b). The calculation is exactly as before, and we discover that the current in the feedback resistor is now 39.7 mA. So R_P needs to provide the load current of 20 mA and an additional 40 mA or so in the feedback path, while the voltage across it is 5 V. This would require R_P = 83 Ω. In practice, it should be slightly lower to prevent slew rate limiting the fall time. Also, the feedback resistor will be raised from 125 Ω to 133 Ω to make up for the finite gain of the AD5539 under these heavily-loaded conditions. If we take the parallel sum of the 50 Ω load, the 70 Ω pull-down and about 150 Ω effective feedback resistance, the actual load on the amplifier is only 24 Ω!

The AD5539 is stable for uncompensated gains of greater than 5, and the AD5539 in this circuit is operating at a gain of just over 3. The 0.01 μF and 10 Ω network compensates by throwing away enough open loop gain to be stable when driving a 50 Ω load. For higher impedance loads, the 10 Ω compensation resistor may need to be reduced.



a.



b.

Figure 9. Equivalent Circuits for Calculating the Value of the Pull-Down Resistor

A level-shifting network is included between the nodes W1 and W2, whose average voltage is about +4 V, to the input of the AD5539 which must be close to ground. With the values shown, the op amp inputs are set slightly below ground (about −460 mV). This network halves the low frequency open-loop gain, which has some effect on the dc accuracy in the presence of offset voltages at the input to the AD5539. If output offset is important, a 500 Ω potentiometer should be inserted in series with the 3.74 kΩ resistors and its slider taken to −6 V. It is then adjusted for zero output with both X and Y inputs set to zero.

Note also that the "inner" Pins X1 and Y2 on the AD834 are grounded to minimize HF feedthrough; the resulting phase-reversal at the X input is corrected by swapping W1 and W2.

Figure 10 shows the pulse response with the input pulse applied to the X input and the Y input set to +1 V, indicating a rise time of 6 ns.

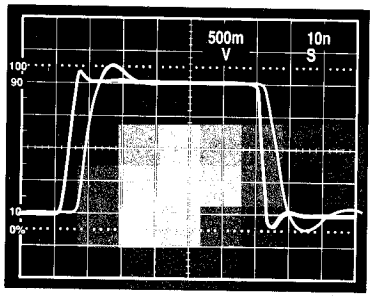


Figure 10. Pulse Response of the DC to 60 MHz Voltage-Controlled Amplifier

Figure 11 shows a set of frequency responses taken on an HP8753B network analyzer for Y inputs of +1 V, 316 mV, +100 mV, and 0 V. In the case of 0 V, the Y input is adjusted to null the input offsets. Note that the high frequency feedthrough is less than −65 dB of full scale (f < 3 MHz).

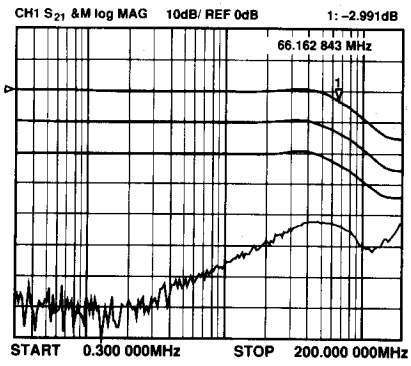


Figure 11. Frequency Response of the DC to 60 MHz Voltage-Controlled Amplifier

A DC TO 480 MHz VOLTAGE-CONTROLLED AMPLIFIER USING ACTIVE LEVEL SHIFTING

Figure 12 (a) shows an active level shifter, using a PNP transistor as a common base stage or cascode. Here, the AD834 is modeled by three ideal current sources, two for the 8.5 mA bias currents and one for the ±4 mA differential signal current. The transistors' bases are tied to +5 V, setting the emitter potential stays at 5.7 V resulting in a voltage of 3.3 V across the resistors R1 and R2 in the absence of signal. Figure 12 (b) shows an equivalent circuit.

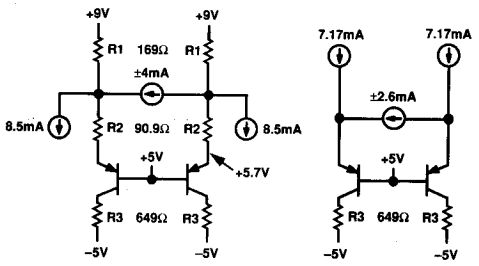


Figure 12. An AD834 Output Stage Using Active Level Shifting

The equivalent dc bias current of 7.17 mA is found by solving for the current flowing into the emitter when the signal current generator is zero. In the ac domain, the signal current generator sees R1 and R2 both tied to low impedance nodes. By inspection, the original signal current has been scaled by:

$$\pm 2.6mA = \pm 4\ mA \times \frac{R1}{R1 + R2} \quad (4)$$

Since AD834's outputs have very high output impedances, the equivalent series resistance can be ignored. The entire 7.17 mA flowing into the cascode's emitter flows out the cascode's collector, assuming a good α, and across R3. The voltage across R3 is:

$$4.65\ V = 7.17\ mA \times 649\ \Omega \quad (5)$$

The operational amplifier's inputs are 350 mV below ground and are within the common-mode range of a wideband amplifier.

The bandwidth of a transistor configured as a cascode is the unity gain frequency (f_T) of the transistor, provided that the user does not create any spurious poles. Choosing an R1 and R2 such that their parallel sum is too large for the transistor's parasitic emitter-base capacitance or an R3 too large for the transistor's parasitic collector-base capacitance will create unwanted poles that lower the frequency response of the circuit.

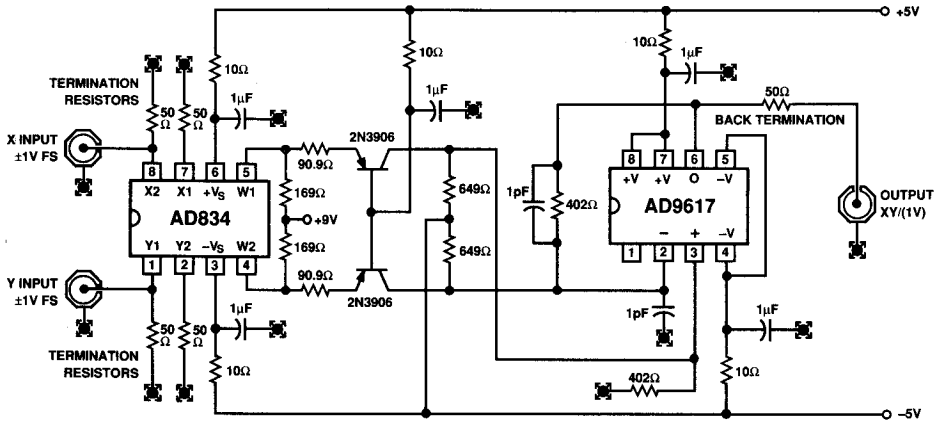


Figure 13. A DC to 480 MHz Voltage-Controlled Amplifier Using Active Level Shifting

Another potential pitfall when using the active PNP level shifter is oscillations at the cascode's emitter. The input impedance of a bipolar junction transistor's emitter is inductive at frequencies approaching its gain-bandwidth product (f_T), while the AD834's output is capacitive. Due to the high bandwidth of the system, these impedances can lead to oscillation.

To prevent such oscillations, the emitter in Figure 12 has been isolated from the AD834's output by R2. This prevents oscillations while providing signal attenuation (gain control) as related in Equation 4. The 2N3906s provide wideband level shifting without resonance or oscillation. Care must be taken when using alternative transistors.

The signal current at the cascodes' collectors is now fed to a wideband amplifier in a differential current to voltage converter configuration as shown in Figure 13. This configuration is similar to an op amp driven current-to-voltage converter which typically follows a current output multiplying digital-to-analog converter.

The AD9617 makes an excellent choice to drive the current to voltage converter. The AD9617 is a second-generation transimpedance amplifier (also known as a current feedback or TZ amplifier) with a fully complementary output stage (unlike the AD5539), and optimized for use with a 400 Ω feedback resistor.

The AD9617 inputs are tied directly to the collectors of the cascodes. The op amp creates a virtual short between the input nodes, forcing all the signal current to flow in the feedback paths. The differential transresistance of the convertor is 400 Ω. The desired scaling can be attained by means of the R1 and R2 attenuation network described above. The full-scale gain of the circuit (X = Y = 1 V) at the AD9617's output is calculated as:

$$2 \times 2.6\,mA \times 400\,\Omega = 2.08\,V \qquad (6)$$

or 1.04 V after the reverse termination resistor. The actual circuit shows a full-scale gain closer to unity.

Figure 14 shows the full-scale step response (−1 V to +1 V) applied to the X input and the Y input set to +1 V demonstrating the circuit's capabilities with a rise time of under 2 ns while exhibiting some overshoot, but no ringing. Note that the output slews at over 500 V/μs.

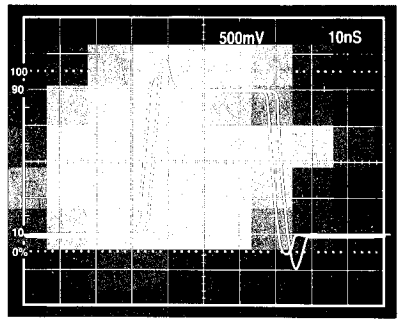


Figure 14. Step Response of the Wideband VCA

Figure 15 shows a set of frequency responses taken on the HP8753B network analyzer for Y inputs of +1 V, 316 mV, +100 mV, and 0 V. The Y input is actually adjusted to null the input offsets. Note that the circuit has a small-signal bandwidth of 500 MHz (at an input power level of 0 dBm). This bandwidth is possible with the two 1 pF capacitors at the inverting node. The high frequency feedthrough is less than −80 dB of full-scale (f < 2 MHz).

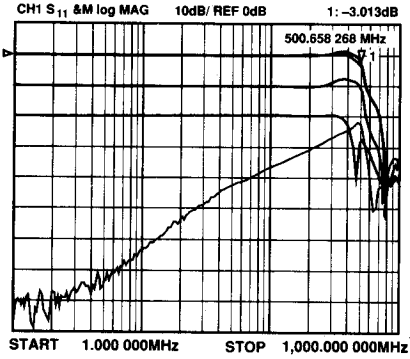


Figure 15. Frequency Response of the Wideband VCA

THE AD834 AS A VIDEO SWITCH

With 0 V or +1 V applied to the X channel as gate control and the video signal to the Y channel, the AD834 becomes a high-speed video switch. Figure 16 illustrates this idea with a high speed current switching circuit centered around an ECL switch. The current flows through either Q1 or Q2, depending on the input voltage. Current switching ensures fast and clean switching to determined levels (+1 V and ground), and allows the user to over- or under-drive the gate input.

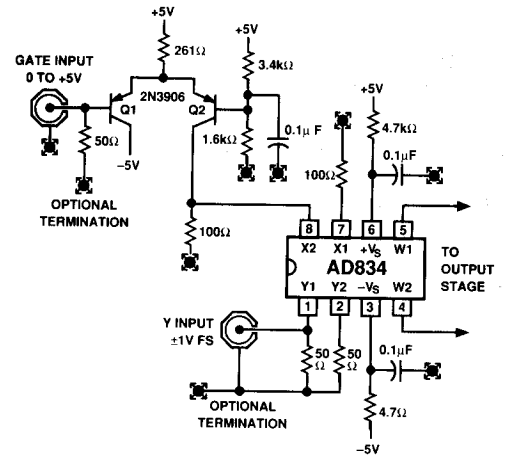


Figure 16. The AD834 as a High-Speed Video Switch

The AD834 switches on as the gate input rises from +1 V through +2 V at the gate circuit input. Below 1 V, Q1 absorbs almost all of the current from the 216 Ω resistor; the 2N3906 transistor is turned off. In this state, the 100 Ω resistor from the X2 input to ground accurately shuts the Y channel off, with Y channel feedthrough to the output measured at −50 dB. With the base of Q2 held at 1.6 V, the transistor's emitter potential is 2.35 V. A steady 10.2 mA (minus base current) from the 261 Ω resistor generates +1 V across the 100 Ω resistor at the X2 input independent of the exact high level of the gate input.

Figure 17 shows a scope photograph of a 1.5 ns rise-time pulse gating a 200 MHz signal. The resulting envelope rise time is 2.7 ns; it has a fall time of 3.0 ns. Although the switched signal may be much slower, the output stage from the AD834 should have a bandwidth greater than 100 MHz in order to maintain an envelope rise time of 3.5 ns.

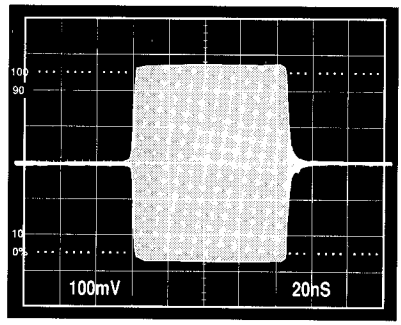


Figure 17. Rise Time of the Video Switch

AC OUTPUT-COUPLING METHODS

In many applications, the dc component at the output can be discarded. In such cases, a wideband buffer can easily ac couple to the AD834 output. The circuits below show the use of simple transformers and baluns for passive, ac coupled output circuits.

TRANSFORMER-COUPLED OUTPUT

Figure 18 shows the use of a center-tapped output transformer, which provides the necessary dc load condition at the outputs W1 and W2, and is designed to match into the desired load impedance by appropriate choice of turns ratio. The specific choice of the transformer design will depend entirely on the application. Transformers may also be used at the inputs. Center-tapped transformers can reduce high frequency distortion and lower HF feedthrough by driving the inputs with balanced signals. Suitable center-tapped transformers include the Coilcraft WB2010PC, which the manufacturer specifies for 0.04 MHz to 250 MHz operation.

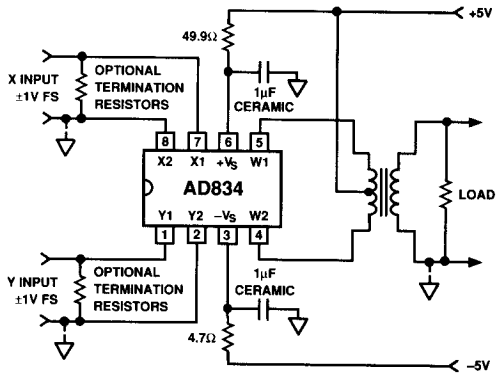


Figure 18. The AD834 with Transformer-Coupled Output

BALUN-COUPLED OUTPUT

Figure 19 shows a circuit which uses blocking capacitors to eliminate the dc offset, and a balun, a particularly effective type of transformer, to convert the differential (or balanced) signal to a single-sided (or unbalanced) output. A balun consists of a short length of transmission line wound on to a toroidal ferrite core, which converts the 'bal'anced output to an 'un'-balanced one (hence the use of the term).

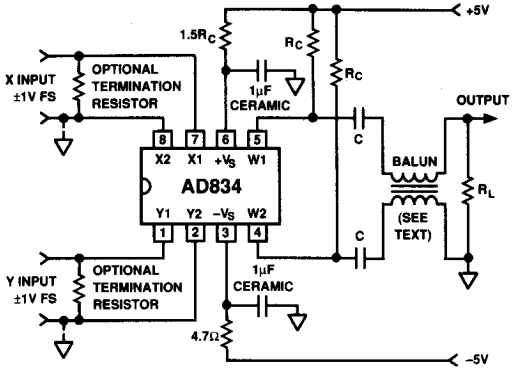


Figure 19. The AD834 with Balun-Coupled Output

Although the symbol used is identical to that for a transformer, the mode of operation is quite different. In the first place, the load should now be equal to the characteristic impedance of the line, although this will usually not be critical for short line lengths. The collector load resistors R_C may also be chosen to reverse-terminate the line, but again this will only be necessary when an electrically long line is used. In most cases, R_C will be made as large as the dc conditions allow, to minimize power loss to the load. The line may be a miniature coaxial cable or a twisted pair.

It is important to note that the upper bandwidth limit of the balun is determined only by the quality of the transmission line; hence, it will usually exceed that of the multiplier. This is unlike a conventional transformer, where the signal is conveyed as a flux in a magnetic core, and is limited by core losses and leakage inductance. The lower limit on bandwidth is determined by the series inductance of the line, taken as a whole, and the load resistance (if the blocking capacitors C are sufficiently large). In practice, a balun can provide excellent differential-to-single-sided conversion over much wider bandwidths than a transformer.

IMPLEMENTATION

Building these circuits requires good high frequency techniques. The circuit schematics suggest suitable layout. **Ground plane is essential for all of the circuits described in this applications brief.** It should cover as much of the component side of the PCB as possible, but not directly underneath the IC or encircling any individual pins. Sockets add to the pin capacitance and inductance, and should be avoided. If sockets are necessary, use individual pin sockets such as AMP p/n 6-330808-3. They contribute far less stray reactance than the molded socket assemblies. Each power trace should be decoupled at the IC with a 0.1 μF low inductance ceramic capacitor, in addition to the main decoupling capacitor. All lead lengths should be kept as short as possible. For lead lengths longer than an inch, stripline techniques should be used.

REFERENCES

[Ref. 1]Gilbert, Barrie, "Translinear Circuits: A Proposed Classification," *Electronic Letters,* Vol. 11, No. 6, pp. 126-127.

[Ref. 2] Gilbert, Barrie, "A Precise Four-Quadrant Multiplier with Subnanosecond Response," *Journal of Solid-State Circuits,* Vol. SC-3, No. 4, pp. 365-373.

[Ref. 3] Gilbert, Barrie, "A New Wideband Amplifier Technique," *Journal of Solid-State Circuits,* Vol. SC-3, No. 4, pp. 353-365.