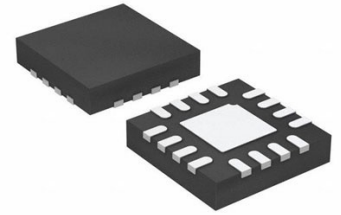



**Clock Generator 0.001MHz to 3.1GHz-IN 3072MHz-OUT 64-Pin
WQFN EP T/R**



Images are for reference only

[Inquiry](#)

Manufacturer:	Texas Instruments, Inc
Package/Case:	WQFN-64
Product Type:	Clock & Timer ICs
RoHS:	RoHS Compliant/Lead free 
Lifecycle:	Active

General Description

The LMK04208 is a high performance clock conditioner with superior clock jitter cleaning, generation, and distribution with advanced features to meet next generation system requirements. The dual loop PLLatinum architecture is capable of 111 fs, RMS jitter (12 kHz to 20 MHz) using a low-noise VCXO module or sub-200 fs rms jitter (12 kHz to 20 MHz) using a low cost external crystal and varactor diode.

The dual loop architecture consists of two high-performance phase-locked loops (PLL), a low-noise crystal oscillator circuit, and a high-performance voltage controlled oscillator (VCO). The first PLL (PLL1) provides low-noise jitter cleaner functionality while the second PLL (PLL2) performs the clock generation. PLL1 can be configured to either work with an external VCXO module or the integrated crystal oscillator with an external tunable crystal and varactor diode. When paired with a very narrow loop bandwidth, PLL1 uses the superior close-in phase noise (offsets below 50 kHz) of the VCXO module or the tunable crystal to clean the input clock. The output of PLL1 is used as the clean input reference to PLL2 where it locks the integrated VCO. The loop bandwidth of PLL2 can be optimized to clean the far-out phase noise (offsets above 50 kHz) where the integrated VCO outperforms the VCXO module or tunable crystal used in PLL1.

Key Features

Ultra-Low RMS Jitter Performance
111 fs, RMS Jitter (12 kHz to 20 MHz)

123 fs, RMS Jitter (100 Hz to 20 MHz)

Dual Loop PLLatinum™ PLL Architecture

PLL1
Integrated Low-Noise Crystal Oscillator Circuit

Holdover Mode when Input Clocks are Lost
Automatic or Manual Triggering/Recovery

PLL2
Normalized PLL Noise Floor of -227 dBc/Hz

Phase Detector Rate of Up to 155 MHz

OSCin Frequency-Doubler

Integrated Low-Noise VCO or External VCO Mode

Two Redundant Input Clocks with LOS
Automatic and Manual Switch-Over Modes

50 % Duty Cycle Output Divides, 1 to 1045 (Even and Odd)

6 LVPECL, LVDS, or LVCMOS Programmable Outputs

Digital Delay: Fixed or Dynamically Adjustable

25 ps Step Analog Delay Control

7 Differential Outputs, Up to 14 Single-Ended
Up to 6 VCXO/Crystal Buffered Outputs

Clock Rates of Up to 1536 MHz

0-Delay Mode

Three Default Clock Outputs at Power Up

Multi-Mode: Dual PLL, Single PLL, and Clock Distribution

Industrial Temperature Range: -40°C to $+85^{\circ}\text{C}$

3.15-V to 3.45-V Operation

64-Pin WQFN Package ($9.0 \times 9.0 \times 0.8$ mm)

Recommended For You

LMK00334RTVR

Texas Instruments, Inc

WQFN32

LMC555CM

Texas Instruments, Inc

SOP8

LM555CM

Texas Instruments, Inc

SOP8

LMC555CMX/NOPB

Texas Instruments, Inc
SOP8

LM555CN

Texas Instruments, Inc
DIP8

LM555J/883

Texas Instruments, Inc
CDIP8

LMC555CMMX

Texas Instruments, Inc
MSOP8

LM555CN/NOPB

Texas Instruments, Inc
DIP8

LMC555CMMX/NOPB

Texas Instruments, Inc
VSSOP8

LMK00101SQE/NOPB

Texas Instruments, Inc
WQFN32

LM555H/883

Texas Instruments, Inc
CAN

LMK1C1102DQFR

Texas Instruments, Inc
WSO8-8

LMC555CN

Texas Instruments, Inc
DIP

LMC555IMX/NOPB

Texas Instruments, Inc
SOP8

LMC555CTP

Texas Instruments, Inc
DSBGA