Functional Safety Information

TIC10024-Q1 and TIC12400-Q1 Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

List of Figures

List of Tables

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1 Overview

This document contains information for the TIC12400-Q1 (TSSOP package) and TIC10024-Q1 (TSSOP package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

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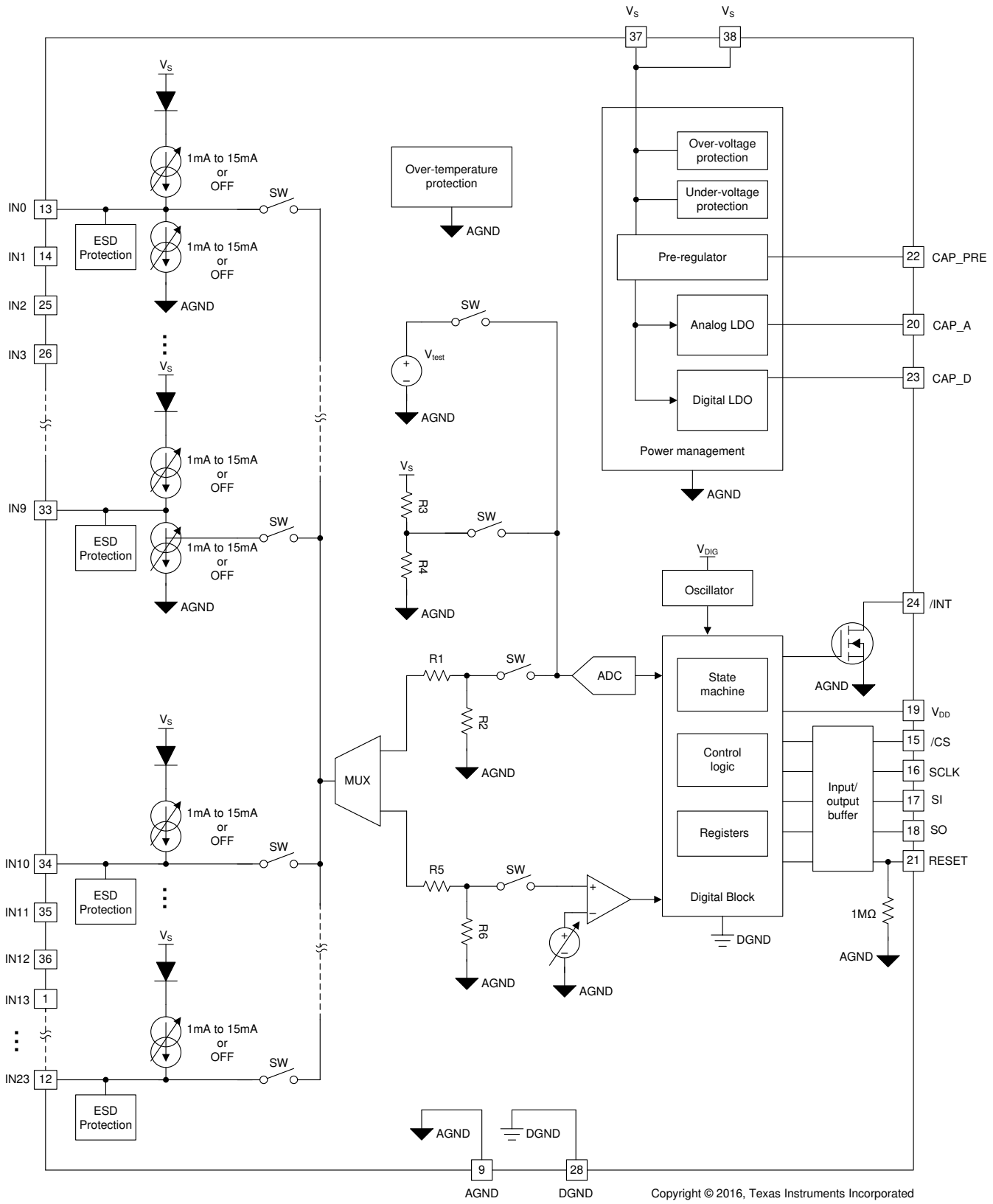

Figure 1-1. Functional Block Diagram

The TIC12400-Q1 and TIC10024-Q1 were both developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TIC12400-Q1 and TIC10024-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	22
Die FIT rate	3
Package FIT rate	19

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: motor control from table 11
- Power dissipation: 3.6 mW
- Climate type: world-wide table 8
- Package factor (lambda 3): table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	60 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TIC12400-Q1 and TIC10024-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Monitoring System and Protection Error	62
Detection Error	18
Power Management Failure	11
Logic Blocks and Clock Failure	7
Communication Error	2

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TIC12400-Q1 and TIC10024-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VS. (see Table 4-5)
- Pin short-circuited to VDD. (see Table 4-6)

Table 4-2 through Table 4-6 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TIC12400-Q1 and TIC10024-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TIC12400-Q1 or the TIC10024-Q1 data sheet.

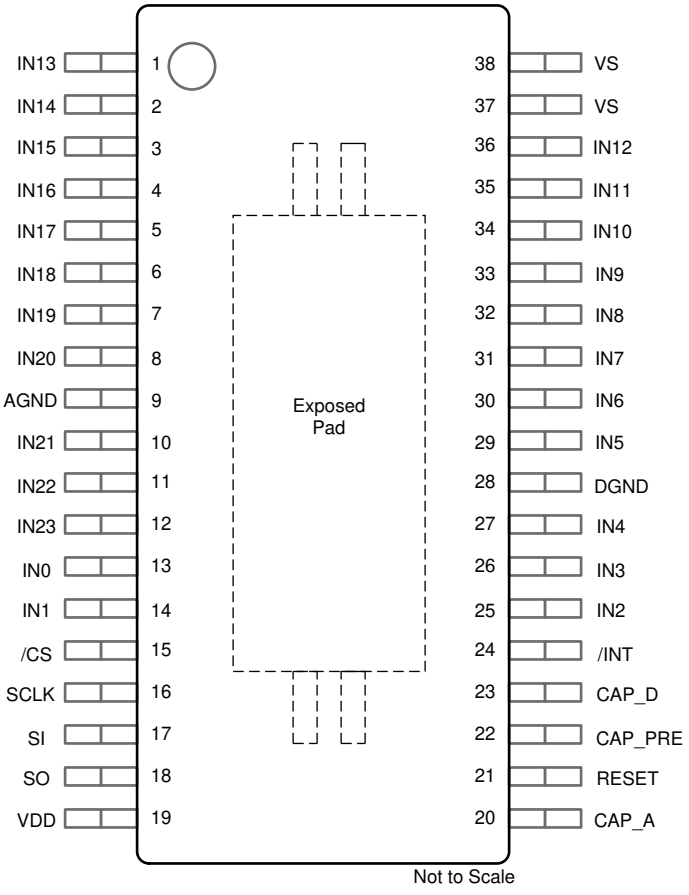

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section

- All device parameters are within the recommended operating conditions of the datasheet.
  - VDD: 3 V to 5.5 V

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– VS: 4.5 V to 35 V

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN13	1	No device damage, this pin is meant to monitor a switch connected to GND. The switch input will be unable to determine state change.	B
IN14	2	No device damage, this pin is meant to monitor a switch connected to GND. The switch input will be unable to determine state change.	B
IN15	3	No device damage, this pin is meant to monitor a switch connected to GND. The switch input will be unable to determine state change.	B
IN16	4	No device damage, this pin is meant to monitor a switch connected to GND. The switch input will be unable to determine state change.	B
IN17	5	No device damage, this pin is meant to monitor a switch connected to GND. The switch input will be unable to determine state change.	B
IN18	6	No device damage, this pin is meant to monitor a switch connected to GND. The switch input will be unable to determine state change.	B
IN19	7	No device damage, this pin is meant to monitor a switch connected to GND. The switch input will be unable to determine state change.	B
IN20	8	No device damage, this pin is meant to monitor a switch connected to GND. The switch input will be unable to determine state change.	B
AGND	9	No effect, this is the intended connected for this pin.	D
IN21	10	No device damage, this pin is meant to monitor a switch connected to GND. The switch input will be unable to determine state change.	B
IN22	11	No device damage, this pin is meant to monitor a switch connected to GND. The switch input will be unable to determine state change.	B
IN23	12	No device damage, this pin is meant to monitor a switch connected to GND. The switch input will be unable to determine state change.	B
IN0	13	No device damage, if configured to monitor a switch connected to battery and the switch is closed, battery will be shorted to GND which may cause excessive current draw from VS.	B
IN1	14	No device damage, if configured to monitor a switch connected to battery and the switch is closed, battery will be shorted to GND which may cause excessive current draw from VS.	B
/CS	15	Chip select will always be in an active state, and SPI communication will not be possible.	B
SCLK	16	The system clock will stuck in a logic-low state, disabling the ability to latch data into the shift register from the SI pin, and not allowing SO data to be available to the controller.	B
SI	17	The SI pin will be stuck in a logic-low state not allowing for any data from the controller to be sent through SPI to the TIC12400-Q1.	B
SO	18	The SO pin will be stuck in a logic-low state not allowing for communication from the TIC12400-Q1 to the controller to happen.	B
VDD	19	The supply for the SPI communication will be at GND, disabling SPI communication.	B
CAP_A	20	The internal analog LDO will no longer have output capacitance causing the LDO to be unstable, and the internal supply rail will be stuck at 0V. Excessive current will also flow from VS to GND.	B
RESET	21	The device will be permanently in normal operation, so a hardware reset will not be possible.	B
CAP_PRE	22	The internal pre-regulator for both the analog and digital LDOs will no longer have output capacitance. This will cause the pre-regulator to be unstable and the internal supply rail will be stuck at 0V. Excessive current will also flow from VS to GND.	B
CAP_D	23	The internal digital LDO will no longer have output capacitance causing the LDO to be unstable, and the internal supply rail will be stuck at 0V. Excessive current will also flow from VS to GND.	B
/INT	24	The interrupt function will be stuck low, not able to indicate any interrupts including if a switch state changed.	B
IN2	25	No device damage, if configured to monitor a switch connected to battery and the switch is closed, battery will be shorted to GND which may cause excessive current draw from VS.	B
IN3	26	No device damage, if configured to monitor a switch connected to battery and the switch is closed, battery will be shorted to GND which may cause excessive current draw from VS.	B
IN4	27	No device damage, if configured to monitor a switch connected to battery and the switch is closed, battery will be shorted to GND which may cause excessive current draw from VS.	B
DGND	28	No effect, this is the intended connected for this pin.	D

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Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN5	29	No device damage, if configured to monitor a switch connected to battery and the switch is closed, battery will be shorted to GND which may cause excessive current draw from VS.	B
IN6	30	No device damage, if configured to monitor a switch connected to battery and the switch is closed, battery will be shorted to GND which may cause excessive current draw from VS.	B
IN7	31	No device damage, if configured to monitor a switch connected to battery and the switch is closed, battery will be shorted to GND which may cause excessive current draw from VS.	B
IN8	32	No device damage, if configured to monitor a switch connected to battery and the switch is closed, battery will be shorted to GND which may cause excessive current draw from VS.	B
IN9	33	No device damage, if configured to monitor a switch connected to battery and the switch is closed, battery will be shorted to GND which may cause excessive current draw from VS.	B
IN10	34	No device damage, if configured to monitor a switch connected to battery and the switch is closed, battery will be shorted to GND which may cause excessive current draw from VS.	B
IN11	35	No device damage, if configured to monitor a switch connected to battery and the switch is closed, battery will be shorted to GND which may cause excessive current draw from VS.	B
IN12	36	No device damage, if configured to monitor a switch connected to battery and the switch is closed, battery will be shorted to GND which may cause excessive current draw from VS.	B
VS	37	The main chip supply of the device will be at 0V, and excessive current draw from the VS power supply would occur.	B
VS	38	The main chip supply of the device will be at 0V, and excessive current draw from the VS power supply would occur.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN13	1	The switch detection input will not be able to detect if the switch state has changed. Loss of functionality, but no damage.	B
IN14	2	The switch detection input will not be able to detect if the switch state has changed. Loss of functionality, but no damage.	B
IN15	3	The switch detection input will not be able to detect if the switch state has changed. Loss of functionality, but no damage.	B
IN16	4	The switch detection input will not be able to detect if the switch state has changed. Loss of functionality, but no damage.	B
IN17	5	The switch detection input will not be able to detect if the switch state has changed. Loss of functionality, but no damage.	B
IN18	6	The switch detection input will not be able to detect if the switch state has changed. Loss of functionality, but no damage.	B
IN19	7	The switch detection input will not be able to detect if the switch state has changed. Loss of functionality, but no damage.	B
IN20	8	The switch detection input will not be able to detect if the switch state has changed. Loss of functionality, but no damage.	B
AGND	9	Device unpowered.	B
IN21	10	The switch detection input will not be able to detect if the switch state has changed. Loss of functionality, but no damage.	B
IN22	11	The switch detection input will not be able to detect if the switch state has changed. Loss of functionality, but no damage.	B
IN23	12	The switch detection input will not be able to detect if the switch state has changed. Loss of functionality, but no damage.	B
IN0	13	The switch detection input will not be able to detect if the switch state has changed. Loss of functionality, but no damage.	B
IN1	14	The switch detection input will not be able to detect if the switch state has changed. Loss of functionality, but no damage.	B
/CS	15	The SPI controller will not be able to engage the chip select for SPI on MSDI. No SPI communication possible.	B

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Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
SCLK	16	The SPI controller cannot drive the clock signal to correctly sample SPI communication. No SPI communication possible.	B
SI	17	The SPI controller cannot send SPI data to the TIC12400-Q1. No SPI communication possible.	B
SO	18	The TIC12400-Q1 cannot send SPI data to the SPI controller. No SPI communication possible.	B
VDD	19	SPI power supply unpowered, SPI communication will not work, but rest of device will still function correctly.	B
CAP_A	20	The internal analog LDO will have no connection to the output capacitor for stability. Internal analog LDO will not work correctly.	B
RESET	21	No controller will be able to drive the reset function on the device. Reset functionality will not be usable.	B
CAP_PRE	22	The internal pre-regulator will have no connection to the output capacitor for stability. Internal pre-regulator will not work correctly.	B
CAP_D	23	The internal digital LDO will have no connection to the output capacitor for stability. Internal digital LDO will not work correctly.	B
/INT	24	External interrupt indication is not available. Controller connected to the TIC12400-Q1 will not be indicated of any interrupts asserted by the TIC12400-Q1.	B
IN2	25	The switch detection input will not be able to detect if the switch state has changed. Loss of functionality, but no damage.	B
IN3	26	The switch detection input will not be able to detect if the switch state has changed. Loss of functionality, but no damage.	B
IN4	27	The switch detection input will not be able to detect if the switch state has changed. Loss of functionality, but no damage.	B
DGND	28	Device unpowered.	B
IN5	29	The switch detection input will not be able to detect if the switch state has changed. Loss of functionality, but no damage.	B
IN6	30	The switch detection input will not be able to detect if the switch state has changed. Loss of functionality, but no damage.	B
IN7	31	The switch detection input will not be able to detect if the switch state has changed. Loss of functionality, but no damage.	B
IN8	32	The switch detection input will not be able to detect if the switch state has changed. Loss of functionality, but no damage.	B
IN9	33	The switch detection input will not be able to detect if the switch state has changed. Loss of functionality, but no damage.	B
IN10	34	The switch detection input will not be able to detect if the switch state has changed. Loss of functionality, but no damage.	B
IN11	35	The switch detection input will not be able to detect if the switch state has changed. Loss of functionality, but no damage.	B
IN12	36	The switch detection input will not be able to detect if the switch state has changed. Loss of functionality, but no damage.	B
VS	37	Device unpowered.	B
VS	38	Device unpowered.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
IN13	1	IN14	No device damage, both pins have the same function. If they are shorted together, they won't be able to differentiate between the different switches connected to either pin. The state of the switch may not be known.	B
IN14	2	IN15	No device damage, both pins have the same function. If they are shorted together, they won't be able to differentiate between the different switches connected to either pin. The state of the switch may not be known.	B

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Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
IN15	3	IN16	No device damage, both pins have the same function. If they are shorted together, they won't be able to differentiate between the different switches connected to either pin. The state of the switch may not be known.	B
IN16	4	IN17	No device damage, both pins have the same function. If they are shorted together, they won't be able to differentiate between the different switches connected to either pin. The state of the switch may not be known.	B
IN17	5	IN18	No device damage, both pins have the same function. If they are shorted together, they won't be able to differentiate between the different switches connected to either pin. The state of the switch may not be known.	B
IN18	6	IN19	No device damage, both pins have the same function. If they are shorted together, they won't be able to differentiate between the different switches connected to either pin. The state of the switch may not be known.	B
IN19	7	IN20	No device damage, both pins have the same function. If they are shorted together, they won't be able to differentiate between the different switches connected to either pin. The state of the switch may not be known.	B
IN20	8	AGND	No device damage, IN20 is meant to monitor a switch connected to GND. IN20 will be unable to determine state change on the connected switch.	B
AGND	9	IN21	No device damage, IN21 is meant to monitor a switch connected to GND. IN21 will be unable to determine state change on the connected switch.	B
IN21	10	IN22	No device damage, both pins have the same function. If they are shorted together, they won't be able to differentiate between the different switches connected to either pin. The state of the switch may not be known.	B
IN22	11	IN23	No device damage, both pins have the same function. If they are shorted together, they won't be able to differentiate between the different switches connected to either pin. The state of the switch may not be known.	B
IN23	12	IN0	No device damage, both pins have the same function. If they are shorted together, they won't be able to differentiate between the different switches connected to either pin. The state of the switch may not be known.	B
IN0	13	IN1	No device damage, both pins have the same function. If they are shorted together, they won't be able to differentiate between the different switches connected to either pin. The state of the switch may not be known.	B
IN1	14	/CS	Potential pin damage if IN1 is monitoring a switch connected to battery and the switch is closed. The /CS absolute maximum could be violated.	A
/CS	15	SCLK	/CS would engage and disengage over and over if SCLK is being serviced by the clock signal from the SPI controller. SPI communication would not be useable.	B
SCLK	16	SI	SPI communication into the TIC12400-Q1 would not be useable, as the input would be a clock signal that could not be read by the TIC12400-Q1.	B
SI	17	SO	SPI communication would not be functioning with both the input from the controller and the output to the controller communicating the same information.	B
SO	18	VDD	SPI communication from the TIC12400-Q1 to the controller would not be possible because it would be stuck in a logic high state.	B
CAP_A	20	RESET	If RESET is driven high, the internal analog LDO has the potential to become unstable.	B
RESET	21	CAP_PRE	If RESET is driven high, the internal pre-regulator has the potential to become unstable.	B
CAP_PRE	22	CAP_D	No failure effect, but the effective capacitance at both outputs will be a different value.	C
CAP_D	23	/INT	If /INT is pulled up externally, the internal digital LDO has the potential to become unstable.	B
/INT	24	IN2	No device damage, but IN2 will be unable to determine state change on the connected switch, and /INT will not be able to properly indicate a switch state change on another INx input or any other interrupt asserted by the TIC12400-Q1.	B

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Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
IN2	25	IN3	No device damage, both pins have the same function. If they are shorted together, they won't be able to differentiate between the different switches connected to either pin. The state of the switch may not be known.	B
IN3	26	IN4	No device damage, both pins have the same function. If they are shorted together, they won't be able to differentiate between the different switches connected to either pin. The state of the switch may not be known.	B
IN4	27	DGND	No device damage, IN4 is meant to monitor a switch connected to GND. IN4 will be unable to determine state change on the connected switch.	C
DGND	28	IN5	No device damage, IN5 is meant to monitor a switch connected to GND. IN5 will be unable to determine state change on the connected switch.	C
IN5	29	IN6	No device damage, both pins have the same function. If they are shorted together, they won't be able to differentiate between the different switches connected to either pin. The state of the switch may not be known.	B
IN6	30	IN7	No device damage, both pins have the same function. If they are shorted together, they won't be able to differentiate between the different switches connected to either pin. The state of the switch may not be known.	B
IN7	31	IN8	No device damage, both pins have the same function. If they are shorted together, they won't be able to differentiate between the different switches connected to either pin. The state of the switch may not be known.	B
IN8	32	IN9	No device damage, both pins have the same function. If they are shorted together, they won't be able to differentiate between the different switches connected to either pin. The state of the switch may not be known.	B
IN9	33	IN10	No device damage, both pins have the same function. If they are shorted together, they won't be able to differentiate between the different switches connected to either pin. The state of the switch may not be known.	B
IN10	34	IN11	No device damage, both pins have the same function. If they are shorted together, they won't be able to differentiate between the different switches connected to either pin. The state of the switch may not be known.	B
IN11	35	IN12	No device damage, both pins have the same function. If they are shorted together, they won't be able to differentiate between the different switches connected to either pin. The state of the switch may not be known.	B
IN12	36	VS	No device damage, IN12 is meant to monitor a switch connected to battery. IN12 will be unable to determine state change on the connected switch.	B
VS	37	VS	No effect, these pins have the same function.	D

Note

This device includes a thermal pad. All device pins are adjacent to the thermal pad. The device behavior when pins are shorted to the thermal pad depends on which net is connected to the thermal pad.

Table 4-5. Pin FMA for Device Pins Short-Circuited to VS

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN13	1	No device damage, but the switch input will be unable to determine state change.	B
IN14	2	No device damage, but the switch input will be unable to determine state change.	B
IN15	3	No device damage, but the switch input will be unable to determine state change.	B
IN16	4	No device damage, but the switch input will be unable to determine state change.	B
IN17	5	No device damage, but the switch input will be unable to determine state change.	B
IN18	6	No device damage, but the switch input will be unable to determine state change.	B
IN19	7	No device damage, but the switch input will be unable to determine state change.	B
IN20	8	No device damage, but the switch input will be unable to determine state change.	B
AGND	9	The device will be unpowered, potential for high current draw on the VS supply.	B

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Table 4-5. Pin FMA for Device Pins Short-Circuited to VS (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN21	10	No device damage, but the switch input will be unable to determine state change.	B
IN22	11	No device damage, but the switch input will be unable to determine state change.	B
IN23	12	No device damage, but the switch input will be unable to determine state change.	B
IN0	13	No device damage, but the switch input will be unable to determine state change.	B
IN1	14	No device damage, but the switch input will be unable to determine state change.	B
/CS	15	Absolute maximum violation, SPI chip select may be damaged. Unable to communicate through SPI.	A
SCLK	16	Absolute maximum violation, SPI clock may be damaged. Unable to communicate through SPI.	A
SI	17	Absolute maximum violation, SPI input to the TIC12400-Q1 may be damaged. Unable to communicate through SPI	A
SO	18	Absolute maximum violation, SPI output from the TIC12400-Q1 may be damaged. Unable to communicate through SPI	A
VDD	19	Absolute maximum violation, SPI supply pin will be damaged. Unable to communicate through SPI.	A
CAP_A	20	Absolute maximum violation, internal analog LDO may be damaged.	A
RESET	21	Absolute maximum violation, device RESET pin and function may be damaged.	A
CAP_PRE	22	Absolute maximum violation, internal pre-regulator may be damaged.	A
CAP_D	23	Absolute maximum violation, internal digital LDO may be damaged.	A
/INT	24	No deivice damage, but external indication for a switch input changing state will no longer be available while short is present.	B
IN2	25	No device damage, but the switch input will be unable to determine state change.	B
IN3	26	No device damage, but the switch input will be unable to determine state change.	B
IN4	27	No device damage, but the switch input will be unable to determine state change.	B
DGND	28	The device will be unpowered, potential for high current draw on the VS supply.	B
IN5	29	No device damage, but the switch input will be unable to determine state change.	B
IN6	30	No device damage, but the switch input will be unable to determine state change.	B
IN7	31	No device damage, but the switch input will be unable to determine state change.	B
IN8	32	No device damage, but the switch input will be unable to determine state change.	B
IN9	33	No device damage, but the switch input will be unable to determine state change.	B
IN10	34	No device damage, but the switch input will be unable to determine state change.	B
IN11	35	No device damage, but the switch input will be unable to determine state change.	B
IN12	36	No device damage, but the switch input will be unable to determine state change.	B
VS	37	No failure, this is the intended use for this pin.	D
VS	38	No failure, this is the intended use for this pin.	D

Table 4-6. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN13	1	No device damage, but logic voltage bias would interfere with the switch input sensing.	C
IN14	2	No device damage, but logic voltage bias would interfere with the switch input sensing.	C
IN15	3	No device damage, but logic voltage bias would interfere with the switch input sensing.	C
IN16	4	No device damage, but logic voltage bias would interfere with the switch input sensing.	C
IN17	5	No device damage, but logic voltage bias would interfere with the switch input sensing.	C
IN18	6	No device damage, but logic voltage bias would interfere with the switch input sensing.	C
IN19	7	No device damage, but logic voltage bias would interfere with the switch input sensing.	C
IN20	8	No device damage, but logic voltage bias would interfere with the switch input sensing.	C
AGND	9	Supply to SPI will be at ground, SPI will be unpowered. SPI communication not possible.	B

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Table 4-6. Pin FMA for Device Pins Short-Circuited to VDD (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN21	10	No device damage, but logic voltage bias would interfere with the switch input sensing.	C
IN22	11	No device damage, but logic voltage bias would interfere with the switch input sensing.	C
IN23	12	No device damage, but logic voltage bias would interfere with the switch input sensing.	C
IN0	13	No device damage, but logic voltage bias would interfere with the switch input sensing.	C
IN1	14	No device damage, but logic voltage bias would interfere with the switch input sensing.	C
/CS	15	The SPI chip select pin will be stuck in the logic high state. SPI communication cannot be enabled.	B
SCLK	16	The SPI clock will be stuck in a logic high state. SPI data will not be able to be clocked in. SPI communication will not be possible.	B
SI	17	SPI communication from the controller to the TIC12400-Q1 would not be possible because the data in would be stuck in a logic high state.	B
SO	18	SPI communication from the TIC12400-Q1 to the controller would not be possible because it would be stuck in a logic high state.	B
VDD	19	No effect, this is the intended use of this pin.	D
CAP_A	20	Internal analog LDO will be biased to VDD voltage. No device damage but LDO may become unstable.	C
RESET	21	RESET pin will be stuck in a logic high state, keeping the device in a hardware reset state. All functionality will be lost.	B
CAP_PRE	22	Internal pre-regulator will be biased to VDD voltage. No device damage but pre-regulator may become unstable.	C
CAP_D	23	Internal digital LDO will be biased to VDD voltage. Device damage possible, and LDO may become unstable.	A
/INT	24	Interrupt pin will be stuck high and unable to externally indicate a switch input state change.	B
IN2	25	No device damage, but logic voltage bias would interfere with the switch input sensing.	C
IN3	26	No device damage, but logic voltage bias would interfere with the switch input sensing.	C
IN4	27	No device damage, but logic voltage bias would interfere with the switch input sensing.	C
DGND	28	No device damage, but logic voltage bias would interfere with the switch input sensing.	C
IN5	29	No device damage, but logic voltage bias would interfere with the switch input sensing.	C
IN6	30	No device damage, but logic voltage bias would interfere with the switch input sensing.	C
IN7	31	No device damage, but logic voltage bias would interfere with the switch input sensing.	C
IN8	32	No device damage, but logic voltage bias would interfere with the switch input sensing.	C
IN9	33	No device damage, but logic voltage bias would interfere with the switch input sensing.	C
IN10	34	No device damage, but logic voltage bias would interfere with the switch input sensing.	C
IN11	35	No device damage, but logic voltage bias would interfere with the switch input sensing.	C
IN12	36	No device damage, but logic voltage bias would interfere with the switch input sensing.	C
VS	37	Potential absolute maximum violation on VDD pin, SPI supply pin will be damaged. Unable to communicate through SPI.	A
VS	38	Potential absolute maximum violation on VDD pin, SPI supply pin will be damaged. Unable to communicate through SPI.	A

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