EP1810LI-45

CPLD Classic Family 900 Gates 48 Macro Cells 22.2MHz 5V

Images are for reference only

Inquiry

Manufacturer:	Rochester Electronics Incorporated
Package/Case:	PLCC68
Product Type:	Programmable Logic ICs
Lifecycle:	Aftermarket

General Description

The Altera ClassicTM device family offers a solution to high-speed, lowpower logic integration. Fabricated on advanced CMOS technology, Classic devices also have a Turbo-only version, which is described in this data sheet. Classic devices support 100% TTL emulation and can easily integrate multiple PAL- and GAL-type devices with densities ranging from 300 to 900 usable gates. The Classic family provides pin-to-pin logic delays as low as 10 ns and counter frequencies as high as 100 MHz. Classic devices are available in a wide range of packages, including ceramic dual in-line package (CerDIP), plastic dual in-line package (PDIP), plastic J-lead chip carrier (PLCC), ceramic J-lead chip carrier (JLCC), pin-grid array (PGA), and small-outline integrated circuit (SOIC) packages. EPROM-based Classic devices can reduce active power consumption without sacrificing performance. This reduced power consumption makes the Classic family well suited for a wide range of low-power applications. Classic devices are 100% generically tested devices in windowed packages and can be erased with ultra-violet (UV) light, allowing design changes to be implemented quickly.

Classic devices use sum-of-products logic and a programmable register. The sum-of-products logic provides a programmable-AND/fixed-OR structure that can implement logic with up to eight product terms. The programmable register can be individually programmed for D, T, SR, or JK flipflop operation or can be bypassed for combinatorial operation. In addition, macrocell registers can be individually clocked either by a global clock or by any input or feedback path to the AND array.

Altera's proprietary programmable I/O architecture allows the designer to program output and feedback paths for combinatorial or registered operation in both active-high and active-low modes. These features make it possible to implement a variety of logic functions simultaneously. Classic devices are supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The MAX+PLUS II software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and workstationbased EDA tools. The MAX+PLUS II software runs on Windows-based PCs, as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations. These devices also contain on-board logic test circuitry to allow verification of function and AC specifications during standard production flow

Recommended For You

EP610PC-30

Rochester Electronics Incorporated

DIP

EP610PI-30

Rochester Electronics Incorporated

DIP24

EP600IPC-45

Rochester Electronics Incorporated

DIP

EP610LC-15

Rochester Electronics Incorporated

PLCC28

EP610PC-35

Rochester Electronics Incorporated

DIP

EP900IPC-50

Rochester Electronics Incorporated

DIP40

EP610LC-35

Rochester Electronics Incorporated

PLCC

EP910LI-35

Rochester Electronics Incorporated

PLCC

EP610LI-30

Rochester Electronics Incorporated

PLCC

EP610DC-30

Rochester Electronics Incorporated

CWDIP24

EP610PC-25T

Rochester Electronics Incorporated

DIP

EP600IDC-45

Rochester Electronics Incorporated

DIP

EP610DC-25

Rochester Electronics Incorporated

DIP

EP910LC-40

Rochester Electronics Incorporated

PLCC44

EP1800ILC-70

Rochester Electronics Incorporated

PLCC68