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AN-9096

Smart Power Module Motion SPM® 55 Series Application Note

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APPLICATION NOTE

1 Introduction

This application note supports the Motion SPM® 55 series. It should be used in conjunction with Motion SPM 55 datasheets, Fairchild's Motion SPM evaluation board user guides and application notes listed in *Section 8 Related Resources*.

1.1 Design Concept

Motion SPM® 55 series are developed to provide a minimized package and a low power consumption with improved reliability. This is achieved by applying a new 600 V gate-driving high-voltage integrated circuit (HVIC), a new insulated-gate bipolar transistor (IGBT) of advanced silicon technology. Motion SPM 55 achieves reduced board size and improved reliability compared to existing discrete solutions. Target applications are inverterized motor drives for low power motor drives, such as washing machine, air conditioners, refrigerator and etc.

The temperature sensing function is implemented in drive IC to enhance the system reliability. An analog voltage proportional to the temperature of the drive IC is provided for monitoring the module temperature and necessary protections against over-temperature situations. Most customers want to know the exact temperature of power chips because temperature affects the quality, reliability, and longevity of the products. Customers have been using an external NTC thermistor for sensing the temperature of the module or heat-sink. This method doesn't accurately reflect the temperature of power components due to cost, but is simple. The temperature sensing function of the Motion SPM 55 provides more accurately reflects the temperature of power chips.

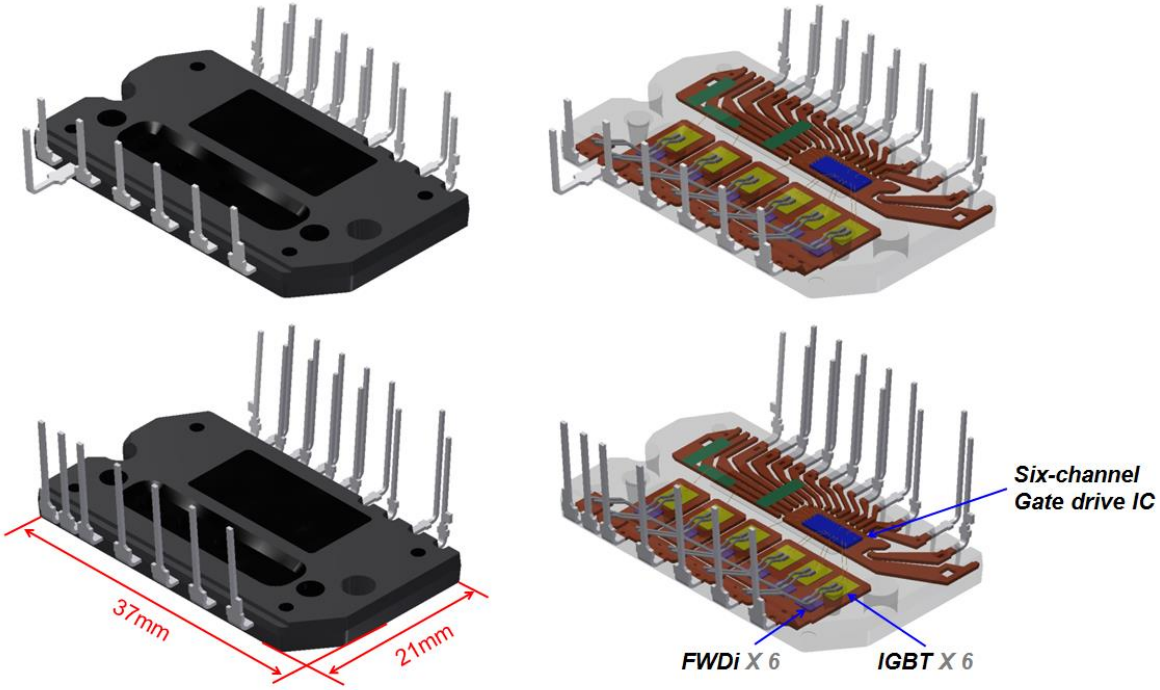


Figure 1. External View and Internal Structure of Motion SPM 55 Series
Top: FNx5xx60T1 (Short Lead Type with Zigzag N-Terminal), Bottom: FNx5xx60T3 (Long Lead Type)

Table 1. Product Line-up and Target Application

Fairchild Device	Type	IGBT Rating	Motor Rating[1]	Target Application	Isolation Voltage
FNB50560Tx	General	5 A / 600 V	0.7 kW	Refrigerator, Fan, Pump, Dish Washer	V_{ISO} = 1500 V_{RMS} (Sine 60 Hz, 1-min All Shorted Pins Heat Sink)
FNA51060Tx	Low $V_{CE(SAT)}$	10 A / 600 V	1.2 kW	Air Conditioner	
FNB51060Tx	Low E_{OFF}	10 A / 600 V		Washing Machine	
FNA51560Tx	Low $V_{CE(SAT)}$	15 A / 600 V	2.0 kW	Air Conditioner	
FNB51560Tx	Low E_{OFF}	15 A / 600 V		Washing Machine	

Notes:
1. These motor ratings are general ratings, so may be changed by conditions.
2. An online loss and temperature simulation tool, Motion Control Design Tool (*https://www.fairchildsemi.com/design/design-tools/motion-control-design-tool/*), is recommended to choose the right SPM product for the application.

1.2 Ordering Information

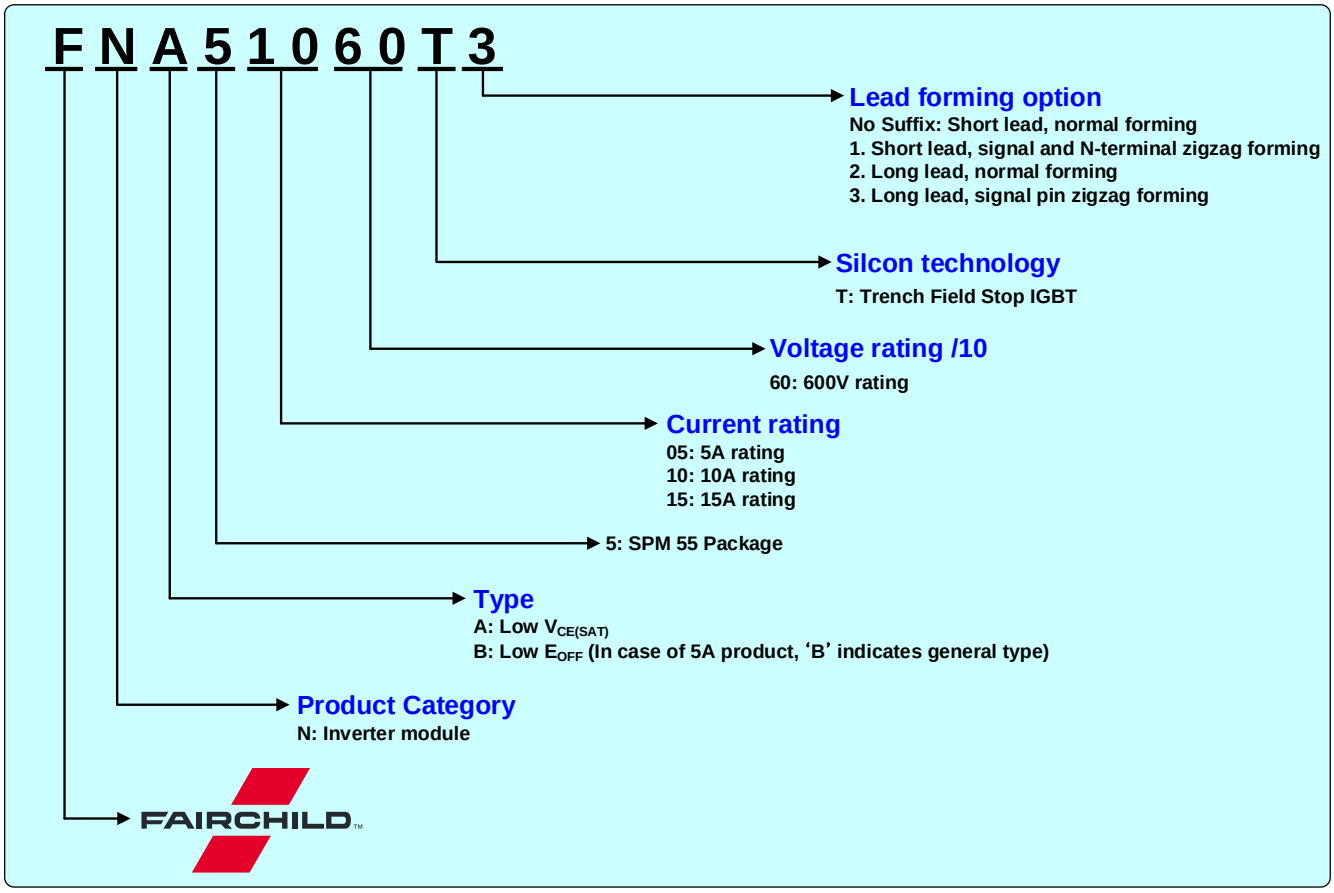


Figure 2. Ordering Information

1.3 Features and Integrated Functions

- Full Mold Package
  - 1500 Vrms Isolation Voltage from Pins to Heat Sink
- Integrated Components:
  - Six-Channel Gate Drive IC for High and Low Side IGBTs Control
  - Six IGBTs / Diodes
- Single DC Supply Compatible Using external Bootstrap Circuit
- Features and Functions
  - Low-Loss, Short-Circuit Rated IGBTs
  - High-Voltage Level-Shift Circuit
  - Input interface: Active HIGH
  - Compatible for 3.3 / 5 V Controller Outputs
  - High Side Under-Voltage Lockout without Fault Signal
  - Low Side Under-Voltage Lockout with Fault Signal
  - Short-Circuit, Over-Current Protection By Detecting Sense Current from External Resistor
  - Temperature Sensing
  - Shut Down Function
  - Inter Lock Function
  - Soft Turn-off to Prevent Excessive Surge Voltage
  - Open Emitter Configuration for Current Sensing of Each Phase

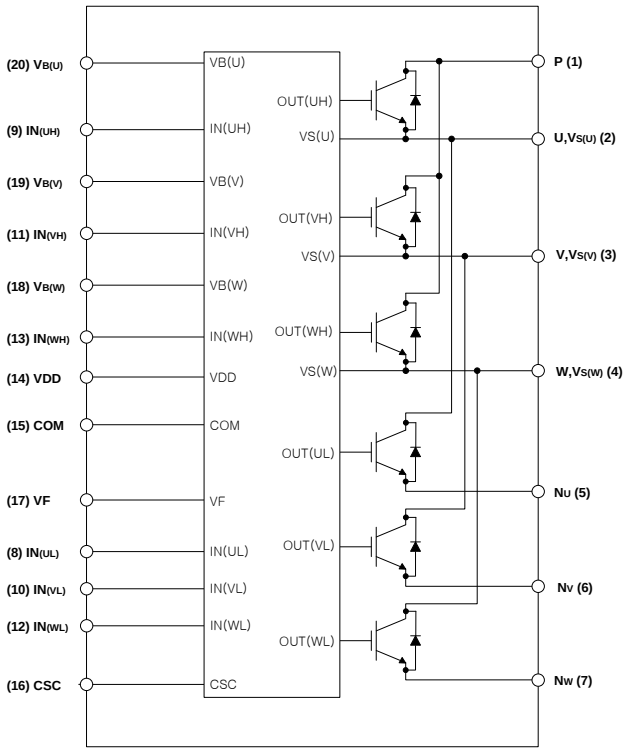


Figure 3. Internal Equivalent Circuit, Input / Output Pins

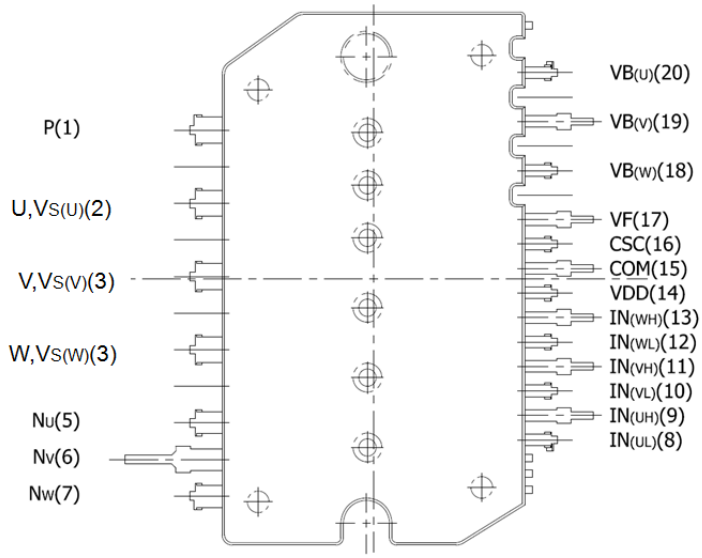


Figure 4. Package Top-View and Pin Assignment (FNx5xx60T1)

2 Product Synopsis

This section discusses pin descriptions, electrical specifications, characteristics, and packaging.

Table 2. Pin Description

Pin Number	Name	Description
1	P	Positive DC Link Input
2	U,$V_{S(U)}$	Output for U Phase
3	V,$V_{S(V)}$	Output for V Phase
4	W,$V_{S(W)}$	Output for W Phase
5	N_U	Negative DC Link Input for U Phase
6	N_V	Negative DC Link Input for V Phase
7	N_W	Negative DC Link Input for W Phase
8	$IN_{(UL)}$	Signal Input for Low-Side U Phase
9	$IN_{(UH)}$	Signal Input for High-Side U Phase
10	$IN_{(VL)}$	Signal Input for Low-Side V Phase
11	$IN_{(VH)}$	Signal Input for High-Side V Phase
12	$IN_{(WL)}$	Signal Input for Low-Side W Phase
13	$IN_{(WH)}$	Signal Input for High-Side W Phase
14	VDD	Common Bias Voltage for IC and IGBTs Driving
15	COM	Common Supply Ground
16	C_{SC}	Shut Down Input for Over Current Protection
17	V_F	Fault Output, Shut Down Input, Temperature Output of Drive IC
18	$V_{B(W)}$	High-Side Bias Voltage for U-Phase IGBT Driving
19	$V_{B(V)}$	High-Side Bias Voltage for V-Phase IGBT Driving
20	$V_{B(U)}$	High-Side Bias Voltage for W-Phase IGBT Driving

2.1 Detailed Pin Definition & Notification

- High-side bias voltage pins for driving the IGBT / high-side bias voltage ground pins for driving the IGBTs:
  - ▶ Pins: $V_{B(U)}$-$V_{S(U)}$, $V_{B(V)}$-$V_{S(V)}$, $V_{B(W)}$-$V_{S(W)}$
  - These are drive power supply pins for providing gate drive power to the high-side IGBTs.
  - The virtue of the ability to bootstrap the circuit scheme is that no external power supplies are required for the high-side IGBTs.
  - Each bootstrap capacitor is charged from the VDD supply during ON state of the corresponding low-side IGBT on and low side diode freewheeling.
  - To prevent malfunctions caused by noise and ripple in the supply voltage, a low-ESR, low-ESL filter capacitor should be mounted very close to these pins.
- Bias voltage pins for gate drive IC:
  - ▶ Pins: VDD
  - This is control supply pins for the built-in gate drive IC.
  - To prevent malfunctions caused by noise and ripple in the supply voltage, a low-ESR, low-ESL filter capacitor should be mounted very close to this pin.
- Low-side common supply ground pin
  - ▶ Pins: COM
  - This is supply ground pin for the built-in gate drive IC.
  - Important! To avoid noise influences, the main power circuit current should not be allowed to blow through this pin.
- Signal input pins
  - ▶ Pins: $IN_{(UH)}$, $IN_{(UL)}$, $IN_{(VH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(WL)}$
  - These pins control the operation of the built-in IGBTs.
  - They are activated by voltage input signals. The terminals are internally connected to a Schmitt-trigger circuit composed of 3.3 / 5 V-class CMOS.
  - The signal logic of these pins is active high. The IGBT associated with each of these pins is turned ON when a sufficient logic voltage is applied to these pins.
  - The wiring of each input should be as short as possible to protect the Motion SPM 55 against noise influences.
  - To prevent signal oscillations, an RC coupling as illustrated in Figure 25 is recommended.
- Short-circuit and over-current detection input pin
  - ▶ Pin: CSC
  - The current detecting resistor should be connected between the CSC and COM pins to detect over-current and short-circuit current (*refer to Figure 17*).
  - The shunt resistor should be selected to meet the detection levels matched for the specific application. An RC filter should be connected to the CSC pin to eliminate noise.
  - The connection length between the shunt resistor and CSC pin should be minimized.
- Fault output / Shut down input / Temperature output
  - ▶ Pin: VF
  - This is multi function pin as fault output, shut down input and temperature output of drive IC
  - Firstly, this is the fault output alarm pin. An active low output is given on this pin for a fault state condition in the motion SPM 55. The alarm conditions are: Short-Circuit Current Protection (SCP), and low-side bias Under-Voltage Lockout (UVLO). The output from VF pin is open drain configured. The signal line of VF pin should be pulled to the 5 V logic power supply with approximately 4.7 kΩ resistance.
  - Secondly, this is the shut down input pin. An active LOW input is given on this pin for the shut down of motion SPM 55 by external control.
  - Thirdly, this pin provides the temperature output of drive IC. Output voltage is determined by pull up voltage, pull up resistor and temperature of drive IC. Positive DC-link pin. Thus, this pin cab be used as a replacement of the thermistor.
- Positive DC-link pin
  - ▶ Pin: P
  - This is the DC-link positive power supply pin of the inverter.
  - It is internally connected to the collectors of the high-side IGBTs.
  - To suppress surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin (tip: metal film capacitor is typically used).
- Negative DC-link pins
  - ▶ Pins: N_U, N_V, N_W
  - These are the DC-link negative power supply pins (power ground) of the inverter. These pins are connected to the low-side IGBT emitters of the each phase.
- Inverter power output pins
  - ▶ Pins: U, V, W
  - Inverter output pins for connecting to the inverter load (e.g. motor).

2.2 Absolute Maximum Ratings

T_J = 25°C, unless otherwise specified.

Table 3. Inverter

Symbol	Parameter	Conditions		Rating	Unit
V_{PN}	Supply Voltage	Applied between P – N_U, N_V, N_W		450	V
$V_{PN(Surge)}$	Supply Voltage (Surge)	Applied between P – N_U, N_V, N_W		500	V
V_{CES}	Collector – Emitter Voltage			600	V
±I_C	Each IGBT Collector Current	T_C=25°C, T_J≤150°C	FNB50560Tx	5	A
			FNA51060Tx	10	
			FNB51060Tx	10	
			FNA51560Tx	15	
			FNB51560Tx	15	
±I_{CP}	Each IGBT Collector Current (Peak)	T_C=25°C, T_J≤150°C, Under 1 ms Pulse Width	FNB50560Tx	10	A
			FNA51060Tx	20	
			FNB51060Tx	20	
			FNA51560Tx	30	
			FNB51560Tx	30	
P_C	Collector Dissipation	T_C=25°C per One Chip	FNB50560Tx	19	W
			FNA51060Tx	22	
			FNB51060Tx	21	
			FNA51560Tx	27	
			FNB51560Tx	22	
T_J	Operating Junction Temperature[3]			-40~150	°C

Note:

3. The maximum junction temperature rating of the power chips integrated within the Motion SPM 55 product is 150°C.

Table 4. Control Part

Symbol	Parameter	Conditions	Rating	Unit
V_{DD}	Control Supply Voltage	Applied between VDD - COM	20	V
V_{BS}	High-Side Control Bias Voltage	Applied between $V_{B(X)}$ – $V_{S(X)}$	20	V
V_{IN}	Input Signal Voltage	Applied between $IN_{(xH)}$, $IN_{(xL)}$ - COM	-0.3~V_{DD}+0.3	V
V_F	Fault Output Supply Voltage	Applied between VF - COM	-0.3~V_{DD}+0.3	V
I_F	Fault Output Current	Sink Current at VF Pin	5	mA
V_{SC}	Current Sensing Input Voltage	Applied between CSC - COM	-0.3~V_{DD}+0.3	V

Table 5. Total System

Symbol	Parameter	Conditions	Rating	Unit
$V_{PN(PROT)}$	Self Protection Supply Voltage Limit (Short-Circuit Protection Capability)	V_{DD}, V_{BS}=13.5~16.5 V, T_J=150°C, Non-Repetitive, < 2 μs	400	V
T_{STG}	Storage Temperature		-40~125	°C
V_{ISO}	Isolation Voltage	60 Hz, Sinusoidal, 1-Minute, Connect Pins to Heat Sink	1500	V_{rms}

Table 6. Thermal Resistance

Symbol	Parameter	Conditions		Rating	Unit
$R_{th(j-c)Q}$	Junction-to-Case Thermal Resistance	Inverter IGBT Part (per 1/6 Module)	FNB50560Tx	6.5	°C/W
			FNA51060Tx	5.6	
			FNB51060Tx	5.9	
			FNA51560Tx	4.55	
			FNB51560Tx	5.6	
$R_{th(j-c)F}$		Inverter FWD Part (per 1/6 Module)	FNB50560Tx	8.9	
			FNA51060Tx	6.9	
			FNB51060Tx	7.6	
			FNA51560Tx	5.4	
			FNB51560Tx	6.9	

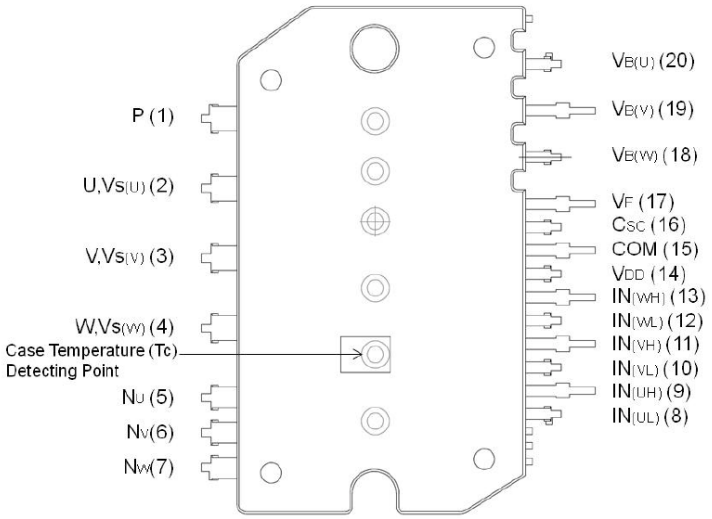


Figure 5. Case Temperature (T_C) Detecting Point (FNx5xx60T1)

Table 7. Recommended Operating Conditions (Based on FNA51560Tx)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{PN}	Supply Voltage	Applied between P - NU, NV, NW		300	400	V
V_{DD}	Control Supply Voltage	Applied between VDD - COM	14.0	15.0	16.5	V
V_{BS}	High-Side Bias Voltage	Applied between $V_{B(X)} – X$, $V_{S(X)}$	13.0	15.0	18.5	V
dV_{DD}/dt, dV_{BS}/dt	Control Supply Variation		-1		+1	V/µs
t_{dead}	Blanking Time for Preventing Arm-Short	For Each Input Signal	1.0			µs
f_{PWM}	PWM Input Signal	$-40°C \le T_C \le 125°C$, $-40°C \le T_J \le 150°C$			20	kHz
V_{SEN}	Voltage for Current Sensing	Applied between N_U, N_V, N_W - COM (Including Surge Voltage)	-4		4	V
$P_{WIN(ON)}$	Minimum Input Pulse Width(4)		1.0			µs
$P_{WIN(OFF)}$			1.0			
T_J	Junction Temperature		-40		150	°C

Note:
4. This product might not make response if the input pulse width is less than the recommended value.

2.3 Electrical Characteristics

T_J = 25°C, unless otherwise specified.

Table 8. Inverter Part (Based on FNA51560Tx)

Symbol		Parameter	Conditions		Min.	Typ.	Max.	Unit
$V_{CE(SAT)}$		Collector–Emitter Saturation Voltage	V_{DD}, V_{BS}=15 V, V_{IN}=5 V, I_C=15 A	T_J=25°C		1.45	1.85	V
				T_J=150°C		1.65		
V_F		FWD Forward Voltage	V_{IN}=0 V, I_F=15 A	T_J=25°C		1.7	2.1	
				T_J=150°C		1.7		
HS	t_{ON}	Switching Times	V_{PN}=600 V, V_{DD} =15 V, V_{BS}=15 V, I_C=15 A T_J=25, V_{IN}=0 V ↔5 V, Inductive Load(5)			700		ns
	$t_{C(ON)}$					140		
	t_{OFF}					850		
	$t_{C(OFF)}$					140		
	t_{rr}					85		
LS	t_{ON}					800		
	$t_{C(ON)}$					250		
	t_{OFF}					850		
	$t_{C(OFF)}$					150		
	t_{rr}					90		
I_{CES}		Collector – Emitter Leakage Current	V_{CE}=V_{CES}				1	mA

Note:

5. t_{ON} and t_{OFF} include the propagation delay of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching times of the IGBT itself under the given gate driving condition internally. *For the detailed information, see Figure 6 and Figure 7.*

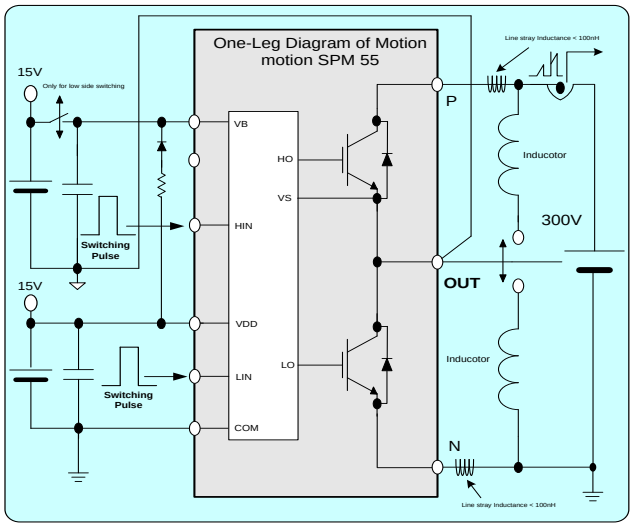


Figure 6. Switching Evaluation Circuit

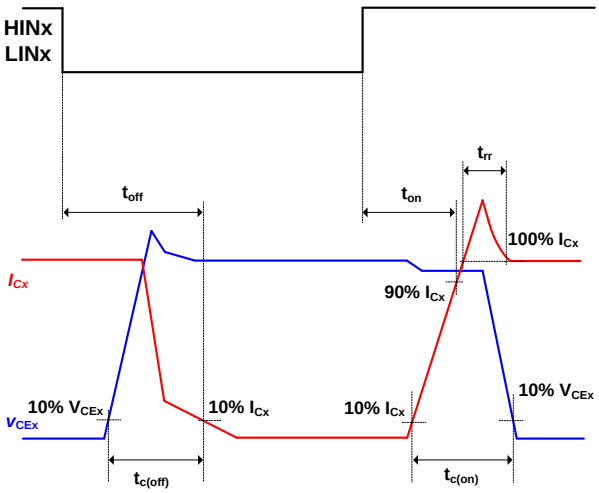


Figure 7. Switching Time Definition

Table 9. Control Part (Based on FNA51560Tx)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{QDD}	Quiescent V_{DD} Supply Current	V_{DD} =15 V, IN(xH), IN(xL)=0 V	VDD - COM			2.6	mA
I_{PDDH}	Operating High-Side V_{DD} Supply Current	V_{DD} =15 V, f_{PWM}=20 kHz, Duty=50%, Applied to One PWM Signal Input for High Side	VDD - COM			3.5	mA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{BS}=15 V, IN(xH)=0 V	Applied between VB(x) –VS(x)			100	μA
I_{PBS}	Operating V_{BS} Supply Current	V_{DD}, V_{BS}=15 V, f_{PWM}=20 kHz, Duty=50%, Applied to One PWM Signal Input for High Side	Applied between VB(x) –VS(x)			800	μA
V_{FH}	Fault Output Voltage	V_{DD}=15 V, V_{SC}=0 V, V_F Circuit: 4.7 kΩ to 5 V Pull-up		4.5			V
V_{FL}		V_{DD}=15 V, V_{SC}=1 V, V_F Circuit: 4.7 kΩ to 5 V Pull-up				0.5	
$V_{SC(ref)}$	Short-Circuit Trip Level	V_{DD}=15 V[6]	CSC - COM	0.45	0.50	0.55	V
UV_{DDD}	Supply Circuit, Under-Voltage Protection	Detection Level		10.0	11.5	13.0	V
UV_{DDR}		Reset Level		10.5	12.0	13.5	
UV_{BSD}		Detection Level		9.5	11.0	12.5	
UV_{BSR}		Reset Level		10.0	11.5	13.0	
V_{TS}	HVIC Temperature Sensing Voltage	V_{DD}=15 V, V_{BS}=15 V, T_{HVIC}=25 ℃		4.44	4.58	4.72	V
t_{FOD}	Fault-Out Pulse Width			40	100		μs
$V_{IN(ON)}$	ON Threshold Voltage	Applied between IN(xH), IN(xL) - COM				2.4	V
$V_{IN(OFF)}$	OFF Threshold Voltage			0.8			

Note:

6. Short-circuit current protection function is for all six IGBTs

3 Package

Since heat dissipation is an important factor in limiting the power module's current capability, the heat dissipation characteristics of a package are important in determining the performance. A trade-off exists among heat dissipation characteristics, package size, and isolation characteristics. The key to good package technology lies in the optimization package size while maintaining outstanding heat dissipation.

In Motion SPM 55, technology was developed with full pack substrate keeping small thickness between lead frame and module case. Power chips are attached directly to the lead frame. Figure 8 and Figure 9 show the package outline and the cross-sections of the Motion SPM 55 package.

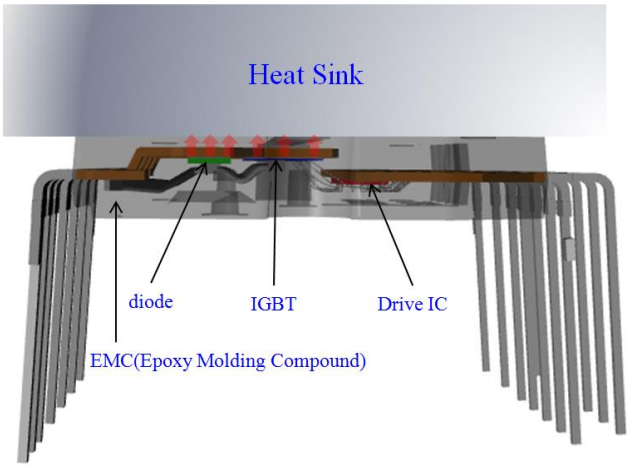


Figure 8. Vertical Structure for Heat Dissipation

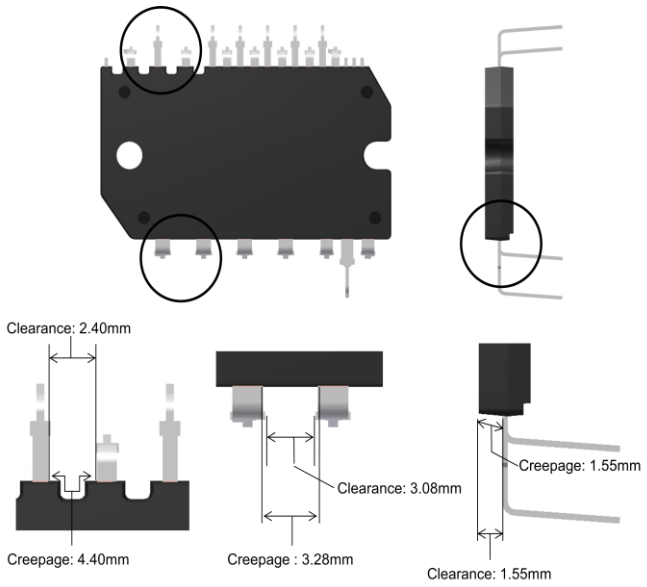


Figure 9. Distance for Isolation from Pin to Pin and from Pins to Heat Sink

Table 10. Mechanical Characteristics and Ratings

Parameter	Conditions		Value			Unit
			Min.	Typ.	Max.	
Device Flatness	*See Figure 10*		-50		100	μm
Mounting Torque	Mounting Screw: M3	Recommended 0.7 N·m	0.6	0.7	0.8	N·m
		Recommended 7.1 kg·cm	5.9	6.9	7.9	kg·cm
Weight				6.0		g

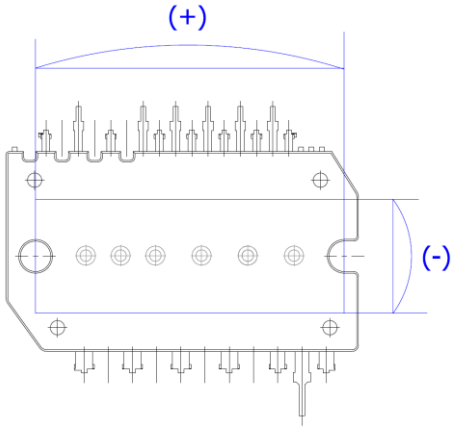
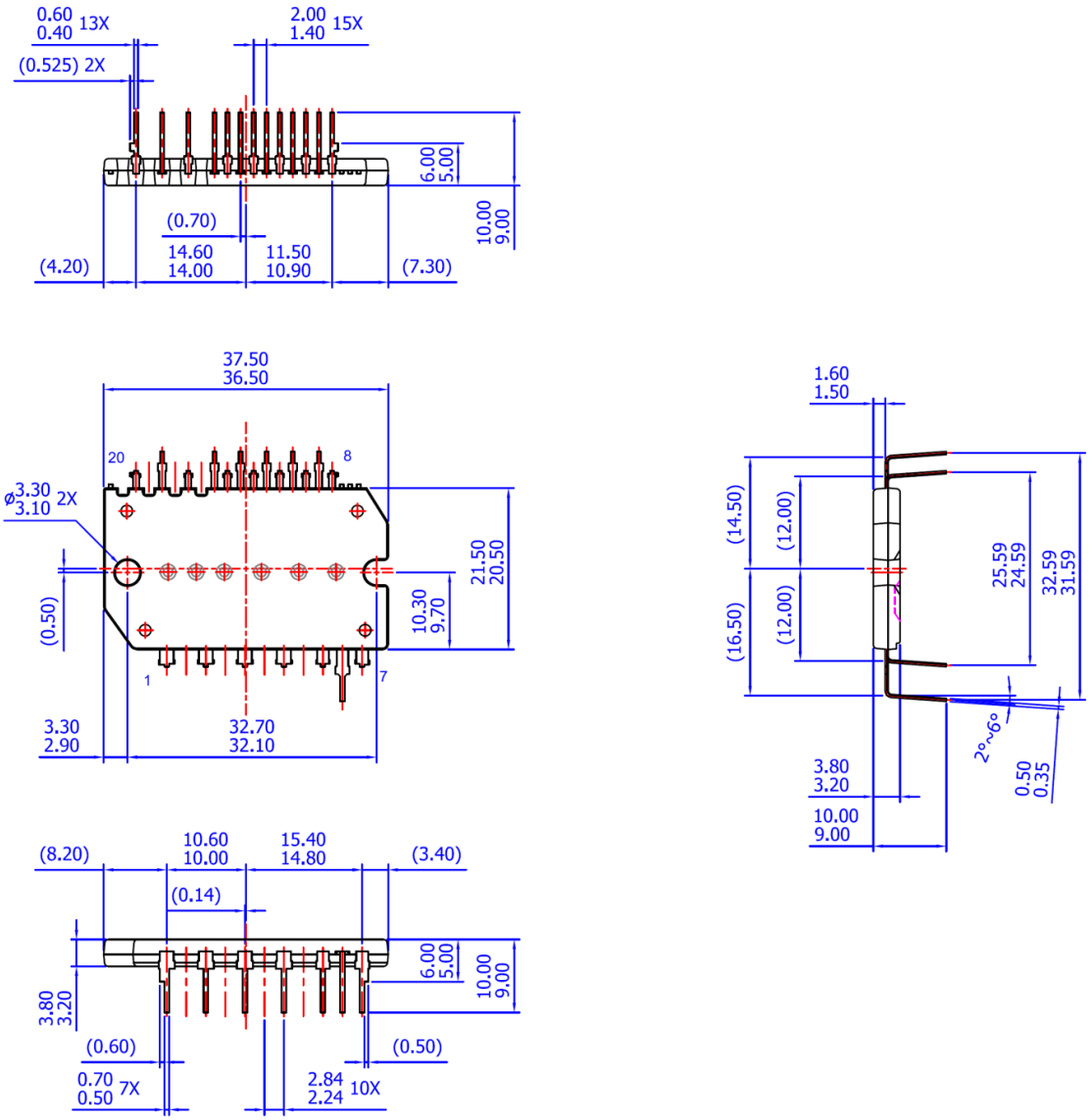


Figure 10. Flatness Measurement Position

3.1 Detailed Package Outline Drawings

FNx5xx60T1, Short Lead



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C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D) ( ) IS REFERENCE
E) [ ] IS ASS'Y QUALITY
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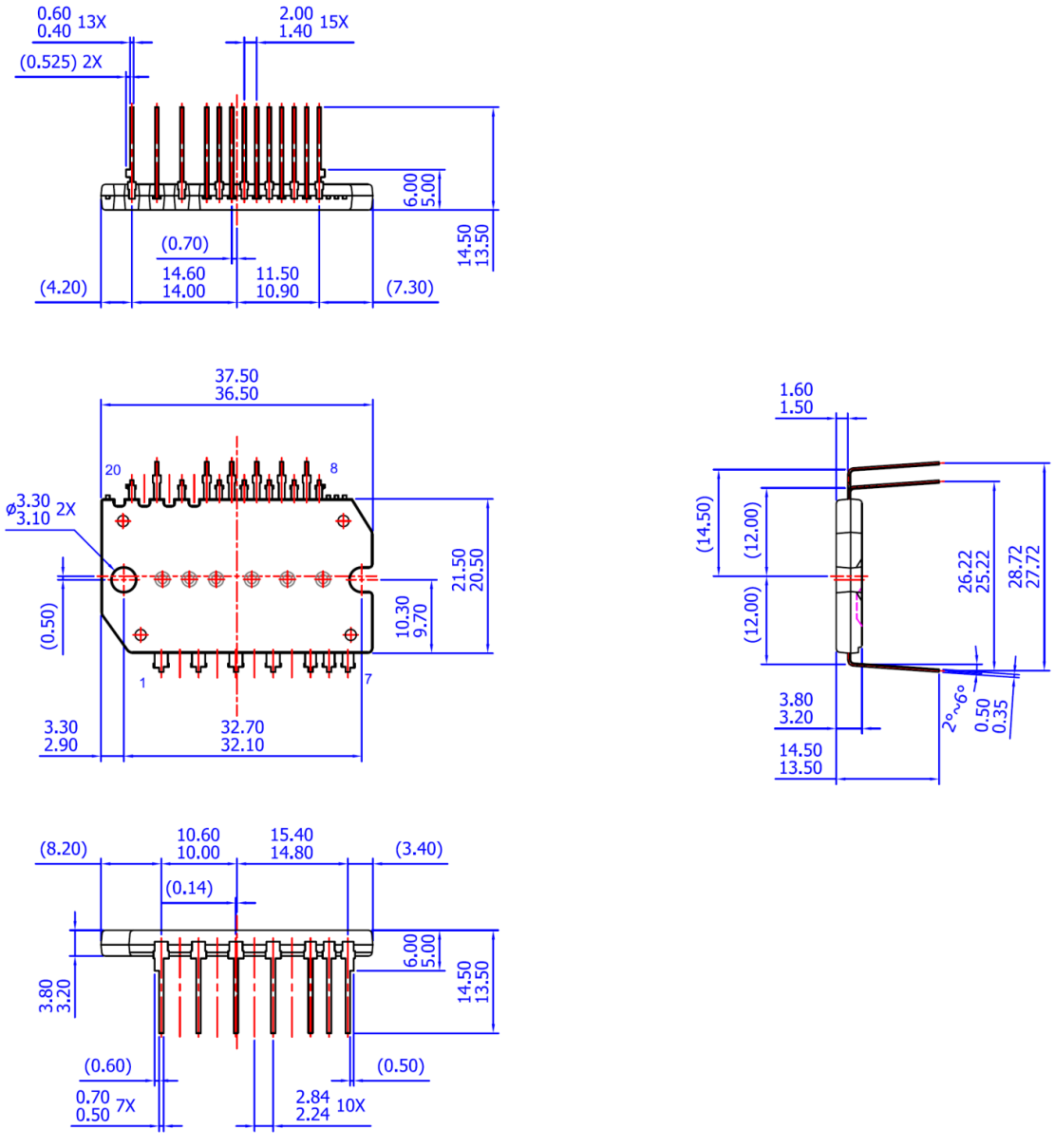
FNx5xx60T3, Long Lead



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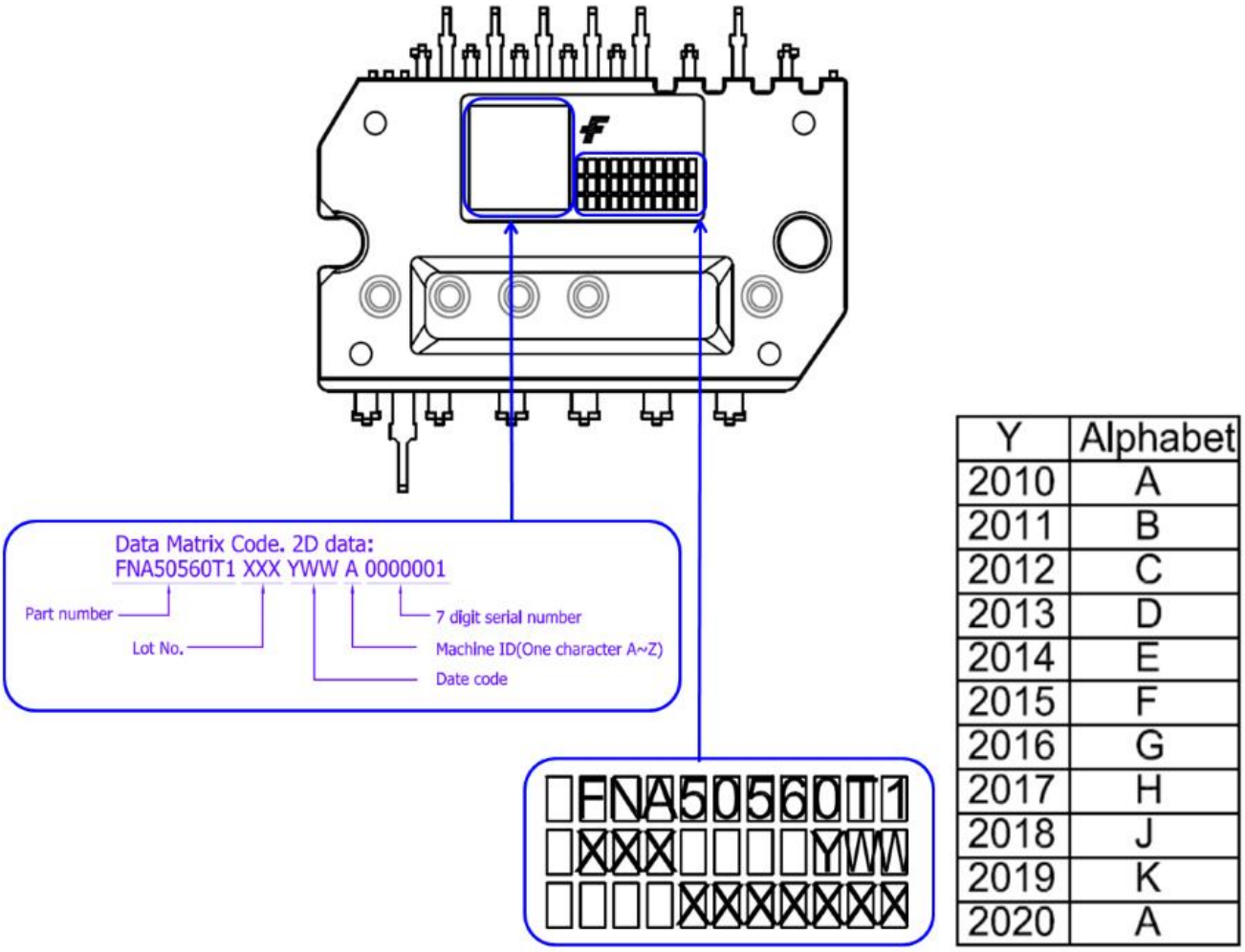
3.2 Marking Information



Y	Alphabet
2010	A
2011	B
2012	C
2013	D
2014	E
2015	F
2016	G
2017	H
2018	J
2019	K
2020	A

* NOTE

1. F : FAIRCHILD LOGO
2. XXX : LAST 3 DIGITS OF LOT NO(OPTION CODE)
3. YWW : WORK WEEK CODE ("Y" REFERS TO THE RIGHT ALPHABET CHARACTER TABLE)

Figure 11. Marking Information

4 Operating Sequence for Protections

4.1 Inter-lock function

Motion SPM 55 provides inter-lock function to prevent leg short circuit by wrong input signal from the controller. Operating timing diagram is shown in Figure 12.

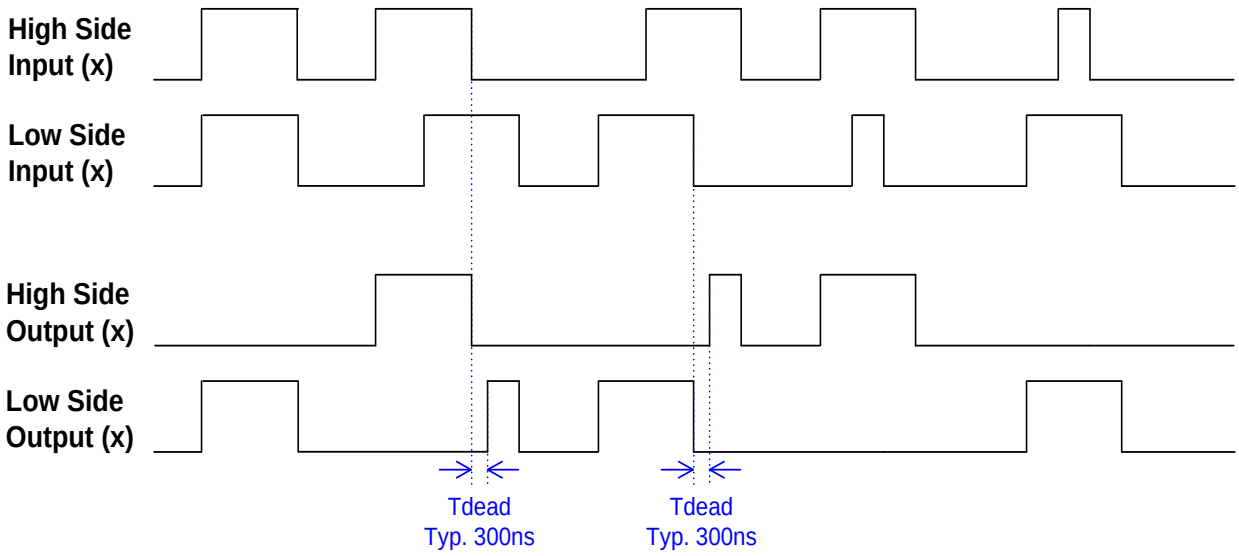


Figure 12. Integrated Gate Drive IC Input / Output Timing Diagram by Inter Lock Function

4.2 Short-Circuit Current Protection (SCP)

Motion SPM 55 uses a external shunt resistor (R_{SC}) for the short circuit current detection, as shown in Figure 13. Drive IC has a built-in short-circuit current protection function. This protection function senses the voltage to the CSC pin. If this voltage exceeds the $V_{SC(ref)}$ (the threshold voltage trip level of the short-circuit) specified in the device datasheets($V_{SC(ref)}$, typ. is 0.5 V), a fault signal is activated to low and the all six IGBTs are turned off. Typically, the maximum short-circuit current magnitude is gate-voltage dependent: higher gate voltage (V_{DD} & V_{BS}) results in larger short-circuit current. To avoid potential problems, the maximum short-circuit trip level is set below 2 times the nominal rated collector current. The drive IC short-circuit current protection-timing chart is shown in Figure 14.

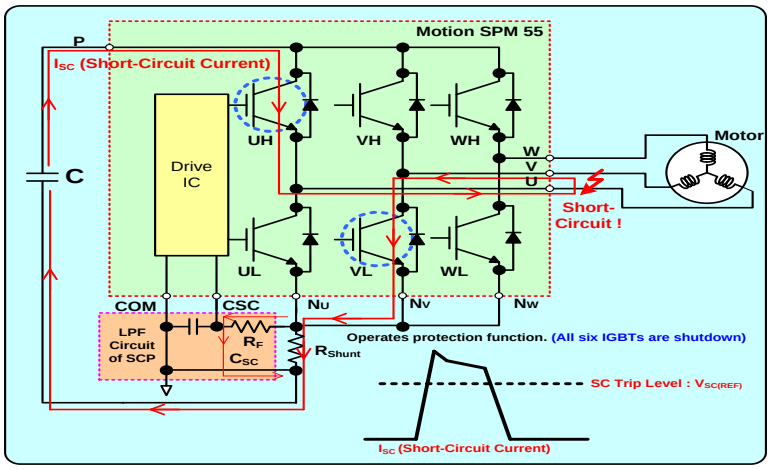


Figure 13. Operation of Short-Circuit Current Protection

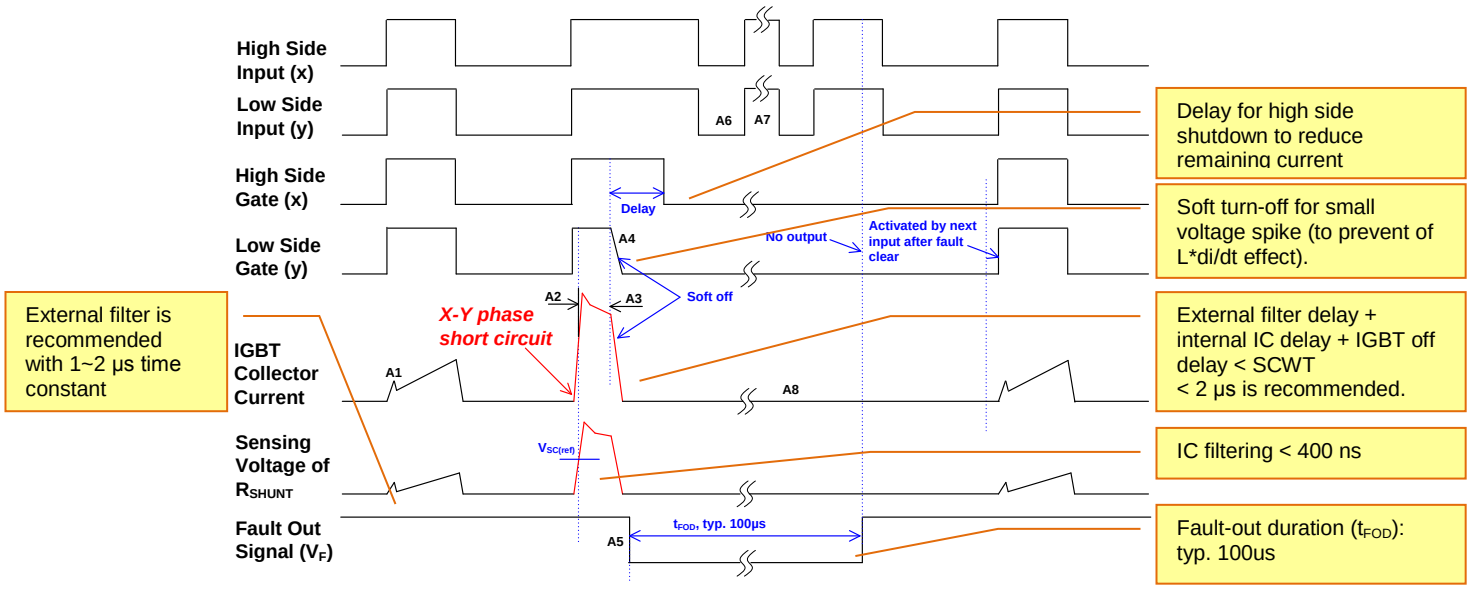


Figure 14. Timing Chart of Short-Circuit Current Protection Function

Notes:

7. A1-normal operation: IGBT on and carrying current.
8. A2-short-circuit current detection (SC trigger).
9. A3-hard IGBT gate interrupt.
10. A4-IGBT turns OFF by soft-off function.
11. A5-fault output timer operation start with internal delay (Typ. 2.0 µs), t_{FOD}=Typ. 100µs.
12. A6-input “L”: IGBT OFF state.
13. A7-input “H”: IGBT ON state, but during the active period of fault output the IGBT doesn’t turn ON.
14. A8-IGBT keeps OFF state.

4.3 Under-Voltage Lockout Protection

The gate drive IC has an under-voltage lockout protection (UVLO) function to protect the low-side IGBTs from operation with insufficient gate driving voltage. A timing chart for this protection is shown in Figure 15.

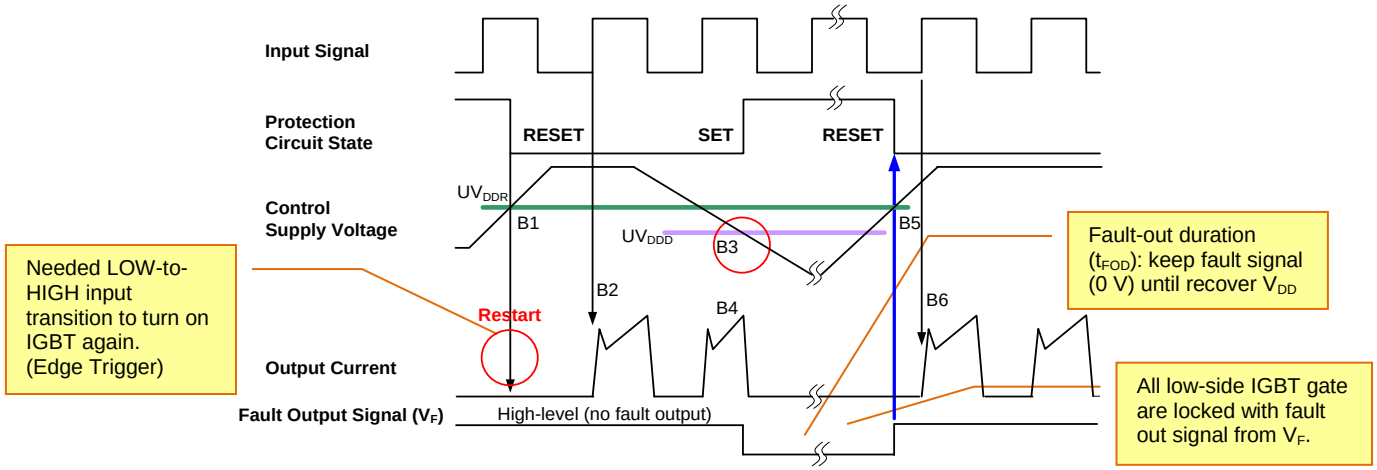


Figure 15. Timing Chart of Low-Side Under-Voltage Protection Function

Notes:

15. B1-control supply voltage rise: after the voltage rises UV_{DDR}, the circuits starts to operate when the next input is applied.
16. B2-normal operation: IGBT ON and carrying current.
17. B3-under-voltage detection (UV_{DDD}).
18. B4-IGBT OFF in spite of control input is alive.
19. B5-fault output signal starts.
20. B6-under-voltage reset (UV_{DDR}).
21. B7-normal operation: IGBT ON and carrying current. If fault-out duration (t_{FOD}) by external capacitor at C_{FOD} pin is longer than UV_{DDR} timing, fault output and IGBT state are cleared after t_{FOD}.

The gate drive IC has an under-voltage lockout function to protect the high-side IGBT from insufficient gate driving voltage. A timing chart for this protection is shown in Figure 16. A fault-out alarm is not given for low at high side bias conditions.

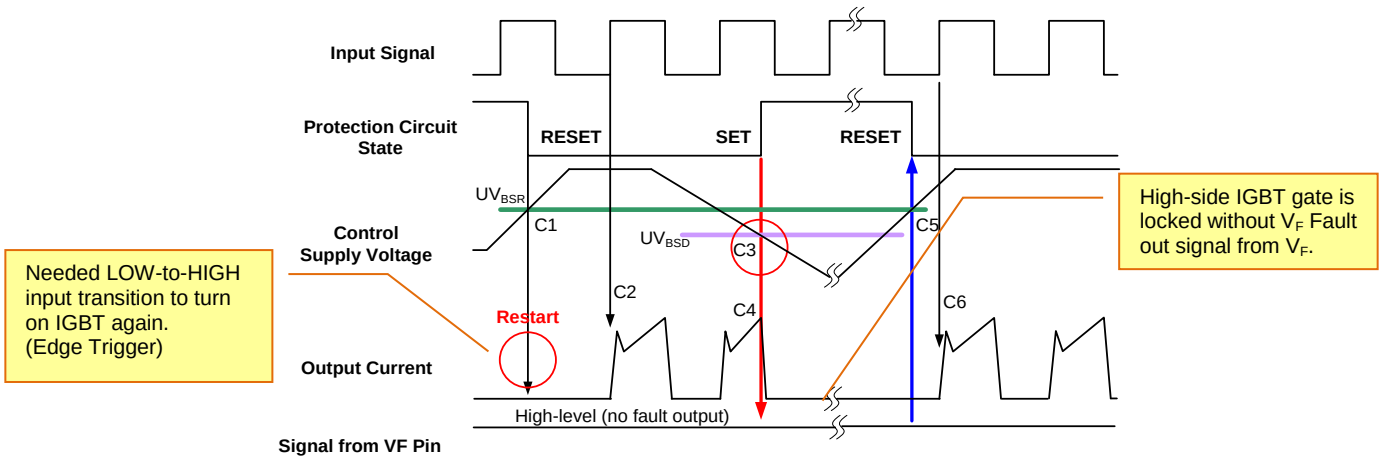


Figure 16. Timing Chart of High-Side Under-Voltage Protection Function

Notes:

22. C1-control supply voltage rises: after the voltage reaches UV_{BSR}, the circuit starts when the next input is applied.
23. C2-normal operation: IGBT ON and carrying current.
24. C3-under-voltage detection (UV_{BSD}).
25. C4-IGBT OFF in spite of control input is alive, but there is no fault output signal.
26. C5-under-voltage reset (UV_{BSR}).
27. C6-normal operation: IGBT ON and carrying current.

5 Key Parameter Design Guidance

For stable operation, there are recommended parameters for passive components and bias conditions, considering operating characteristics of Motion SPM 55 series.

5.1 Shunt Resistor Selection at N-Terminal for Current Sensing & Protection

The external RC time constant from the N-terminal shunt resistor to CSC must be lower than 2 μs when overload condition is detected for a stable shutdown.

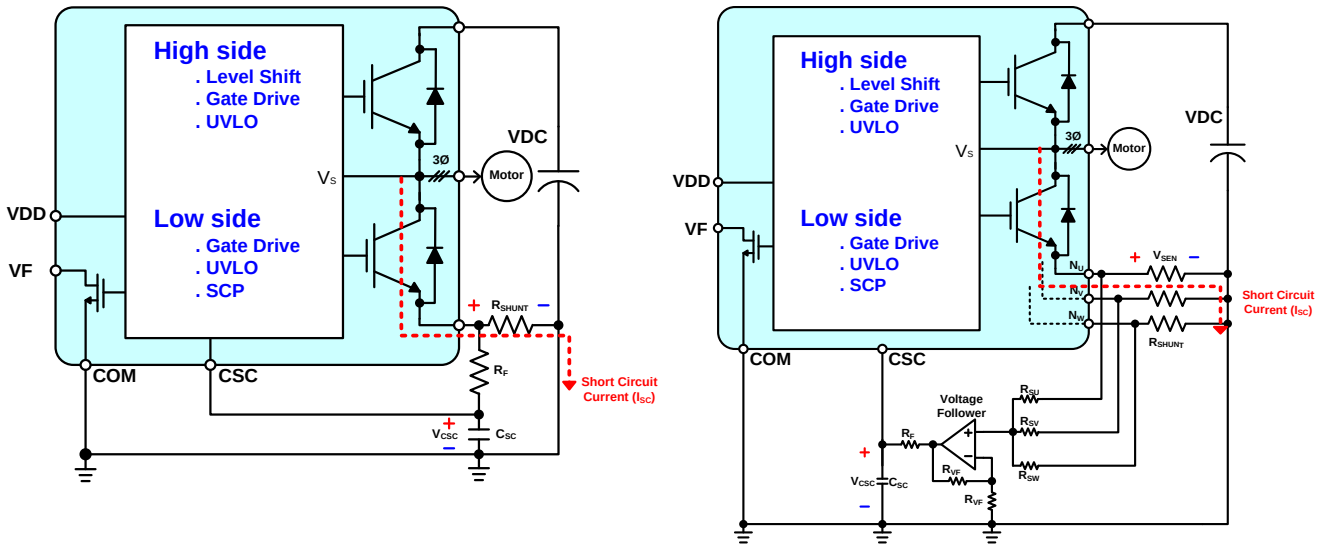


Figure 17. Recommended Circuitry for Over-Current & Short-Circuit Protection

Table 11. OCP & SCP Level ($V_{SC(ref)}$) Specification

Conditions	Min.	Typ.	Max.	Unit
Specification at T_J=25°C, V_{DD}=15 V	0.45	0.50	0.55	V

Table 12. Operating Short-Circuit Current Range (R_{SHUNT}=38 mΩ (Min.), 40 mΩ (Typ.), 42 mΩ (Max.)) *(see the equations below)*

Conditions	Min.	Typ.	Max.	Unit
Operating SC Level at T_J=25°C	10	12	15	A

In case of one shunt, the value of shunt resistor is calculated by the following equations.

Maximum current trip level (depend on user selection):

$$I_{SC(max)} = 1.5 \times I_{C(max)}$$

SC trip reference voltage (depends on datasheet):

$$V_{SC(ref)} = min.\ 0.45V,\ typ.\ 0.5V,\ max.\ 0.55V$$

Shunt resistance:

$$I_{SC(max)} = V_{SC(max)} / R_{SHUNT(min)} \rightarrow R_{SHUNT(min)} = V_{SC(max)} / I_{SC(max)}$$

If the deviation of the shunt resistor is limited below ± 5%:

$$R_{SHUNT(typ)} = R_{SHUNT(min)} / 0.95,$$

$$R_{SHUNT(max)} = R_{SHUNT(typ)} \times 1.05$$

Actual SC trip current level becomes:

$$I_{SC(typ)} = V_{SC(typ)} / R_{SHUNT(typ)},\ I_{SC(min)} = V_{SC(min)} / R_{SHUNT(max)}$$

Inverter output power:

$$P_{OUT} = \frac{\sqrt{3}}{\sqrt{2}} \times MI \times V_{DC\_Link} \times I_{RMS} \times PF$$

where:

MI = Modulation Index;

V_{DC_Link} *= DC link voltage;*

I_{RMS} *= Maximum load current of inverter; and*

PF = Power Factor

Average DC current

$$I_{DC\_AVG} = V_{DC\_Link} / (P_{out} \times Eff)$$

where:

Eff = Inverter efficiency

The power rating of shunt resistor is calculated by the following equation:

$$P_{SHUNT} = (I^2_{DC\_AVG} \times R_{SHUNT} \times Margin) / Derating\ Ratio$$

where:

RSHUNT=Shunt resistor typical value at T_C*=25*°C

Derating Ratio=Derating ratio of shunt resistor at T_{SHUNT}*=100*°C

(From datasheet of shunt resistor); and

Margin = Safety margin (determined by user)

✓ **Shunt Resistor Calculation Examples**

Calculation Conditions:

- DUT: FNA51560Tx
- Tolerance of shunt resistor: ±5%
- SC Trip Reference Voltage:

  $V_{SC(min)}$=0.45 V, $V_{SC(typ)}$=0.50 V, $V_{SC(max)}$=0.55 V
- Maximum Load Current of Inverter (I_{RMS}): 7 A_{rms}
- Maximum Peak Load Current of Inverter ($I_{C(max)}$): 15 A
- Modulation Index(MI) : 0.9
- DC Link Voltage(V_{DC_Link}): 300 V
- Power Factor(PF): 0.8
- Inverter Efficiency(Eff): 0.95
- Shunt Resistor Value at T_C = 25°C (R_{SHUNT}): 25 mΩ
- Derating Ration of Shunt Resistor at T_{SHUNT} = 100°C: 70%
- Safety Margin: 20%
- Calculation Results:
- $I_{SC(max)}$: 1.5 × $I_{C(max)}$ = 1.5 x 15 A = 22.5 A
- $R_{SHUNT(min)}$: $V_{SC(max)}$ / $I_{SC(max)}$=0.55 V / 22.5 A=25 mΩ
- $R_{SHUNT(typ)}$: $R_{SHUNT(min)}$ / 0.95 = 25 mΩ / 0.95 = 26 mΩ
- $R_{SHUNT(max)}$: $R_{SHUNT(typ)}$ x 1.05 = 40.0 mΩ x 1.05 = 28 mΩ
- $I_{SC(min)}$: $V_{SC(min)}$ / $R_{SHUNT(max)}$ = 0.45 V / 28 mΩ = 16.1 A
- $I_{SC(typ)}$: $V_{SC(typ)}$ / $R_{SHUNT(typ)}$ = 0.5 V / 26 mΩ = 19.2 A
- $P_{OUT} = \frac{\sqrt{3}}{\sqrt{2}} \times MI \times V_{DC\_Link} \times I_{RMS} \times PF = \frac{\sqrt{3}}{\sqrt{2}} \times 0.9 \times 300 \times 7 \times 0.8$ = 1852 W
- I_{DC_AVG} = (P_{OUT}/Eff) / V_{DC_Link} = 6.50 A
- P_{SHUNT} = ($I^2_{DC\_AVG}$ × R_{SHUNT} × Margin) / Derating Ratio = (7^2 × 0.026 × 1.2) / 0.7 = 1.88 W (Therefore, the proper power rating of shunt resistor is over 2W)

5.2 Time Constant of Internal Delay

An RC filter prevents noise-related Short-Circuit Current Protection (SCP) circuit malfunction. The RC time constant is determined by the applied noise time and the Short-Circuit Current Withstanding Time (SCWT) of Motion SPM 55. When the R_{SHUNT} voltage exceeds the SCP level, this is applied to the CSC pin via the RC filter. The RC filter delay (T1) is the time required for the CSC pin voltage to rise to the referenced SCP level. The gate drive IC has an internal filter time (logic filter time for noise elimination: T2). Consider this filter time when designing the RC filter of V_{CSC}.

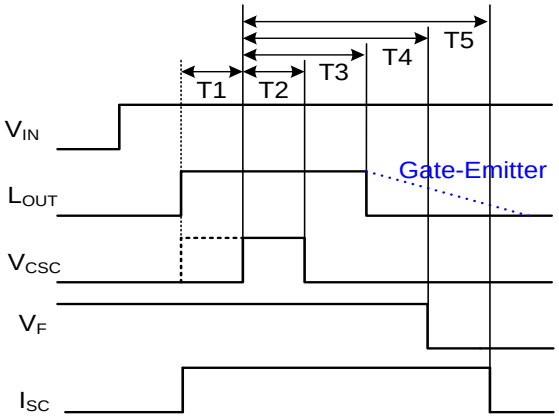


Figure 18. Timing Diagram

Notes:

28. V_{IN}: Voltage of input signal.
29. L_{OUT}: V_{GE} of low-side IGBT.
30. V_{CSC}: Voltage of CSC pin.
31. I_{SC}: Short-circuit current.
32. V_F: Voltage of VF pin.
33. T1: filtering time of RC filter of V_{CSC}.
34. T2: filtering time of CSC. If V_{CSC} width is less than T2, SCP does not operate.
35. T3: delay from CSC triggering to gate-voltage down.
36. T4: delay from CSC triggering to fault-out signal.
37. T5: delay from CSC triggering to short-circuit current.

Table 13. Time Table on Short-Circuit Conditions: V_{CSC} to L_{OUT}, I_{SC}, V_F

Device Under Test	Typ. at T_J=25°C	Max. at T_J=25°C
FNA51560Tx	T2=0.4 µs	Considering ±20% Dispersion, T4=1.6 µs
	T3=0.8 µs	
	T4=1.1 µs	
	T5=1.3 µs	

Notes:

38. To guarantee safe short-circuit protection under all operating conditions, C_{SC} should be triggered within 0.4 µs after short-circuit occurs. (Recommendation: SCWT < 2.0 µs, Conditions: V_{DC}=400 V, V_{DD}=16.5 V, T_J=150°C).
39. It is recommended that delay from short-circuit to CSC triggering should be minimized.

5.3 Soft Turn-Off

A soft turn-off function protects the low side IGBTs from over voltage of V_{PN} (supply voltage) by "hard off at over current or short circuit mode," which is when IGBTs are turned off by short input signal before the SCP function under short-circuit condition. In this case, V_{PN} rapidly rises by fast and large di/dt of I_C (over-current or short-circuit current). This kind of rapid rise of V_{PN} can cause destruction of IGBT by over-voltage. Therefore, soft-off function prevents IGBT rapid turning off by slow discharging of V_{GE} (gate-to-emitter voltage of IGBT).

An internal block diagram of low side and operation sequence of soft turn-off function are shown in Figure 19 and Figure 20. This function operates by two internal protection functions (UVLO and SCP). When the IGBT is turned off in normal conditions, gate drive IC turns off the IGBT immediately by turn-off gate signal ($IN_{(XL)}$) via gate driver block. Pre-driver turn-on output buffer of gate driver block, path ①. When the IGBT is turned off by a protection function, the gate driver is disabled by the protection function signal via output of protection circuit (disable output buffer, high-Z) and output of the protection circuit turn-on switch of the soft-off function. V_{GE} (IGBT gate-emitter voltage) is discharged slowly via circuit of soft-off (path ②).

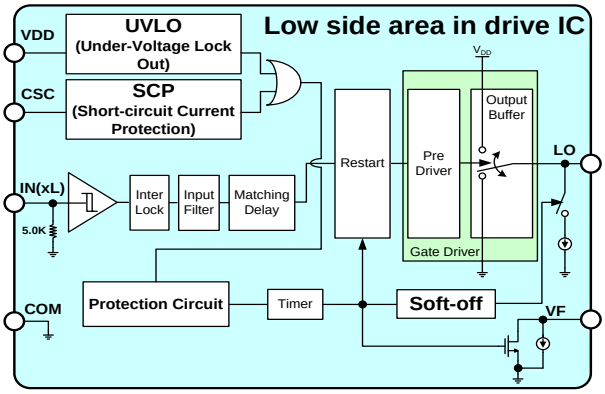


Figure 19. Internal Block Diagram of Gate Drive IC

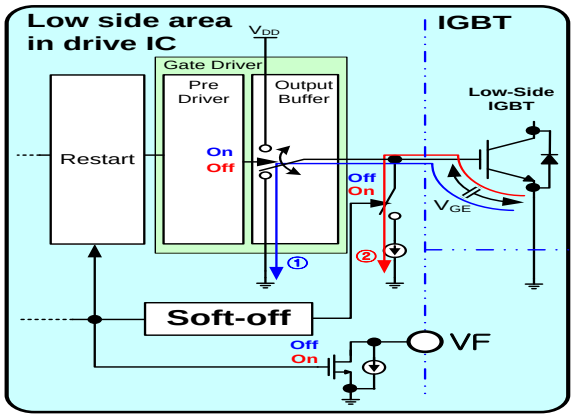


Figure 20. Operating Sequence of Soft Turn-Off

5.4 Multi function pins (VF)

VF terminal provides multi functions which are fault out, shut down input and temperature monitoring. Firstly, VF terminal provides temperature monitoring function for temperature of internal drive IC. As shown in Figure 21, VF terminal is connected to ADC and fault detection terminals of micro controller. This circuit is very simple and IGBTs can be shut down by micro controller. For example, when R1 is 10 kΩ, then V_F at about 110°C of thermistor temperature is 1.96 $V_{typ.}$ at V_{ctr} = 5 V as shown in Figure 22. User can control target voltage simply by change R1 value

It's noted that VF for over temperature protection should be not less than micro controller fault trip level.

Table 14. Maximum Ratings of VF Part

Symbol	Item	Condition	Rating	Unit
V_F	Fault Supply Voltage	Applied between VF-COM	-0.3 ~ V_{DD}+0.3	V
I_F	Fault Current	Sink Current at VF Pin	2	mA

Table 15. Electric Characteristics

Symbol	Item	Conditions	Min.	Max.	Unit
V_{FH}	Fault Voltage	V_{DD}=15 V, V_{SC}=0, V_F Circuit: 4.7 kΩ to 5 V Pull-Up	4.5		V
V_{FL}		V_{DD}=15 V, V_{SC}=1 V, V_F Circuit: 4.7 kΩ to 5 V Pull-Up		0.5	V
I_{FT}	HVIC Temperature Sensing Current	V_{DD}=15 V, T_{HVIC}=25℃	70	120	μA
V_{FT}	HVIC Temperature Sensing Voltage	V_{DD}=15 V, T_{HVIC}=25℃, 4.7 kΩ to 5 V Pull-Up		4.55	V
V_{FSDS}	Shut Down Set Level	Applied between V_F-COM	0.8		V
V_{FSDR}	Shut Down Reset Level			2.4	V

Figure 21 and Figure 22 describe timing diagram of fault out and shut down input functions. Temperature of drive IC in SPM 55 is calculated by below equation.

$$T_{HVIC} = ((Vctr - VF) - 20uA \times R1) / (R1 \times 2.76\mu A)$$

It is noted that above equation is based on 'current = zero' in fault input area of controller. If leakage current exists at fault input of controller, '20 μA' in above equation should be changed to '20 μA + leakage current'.

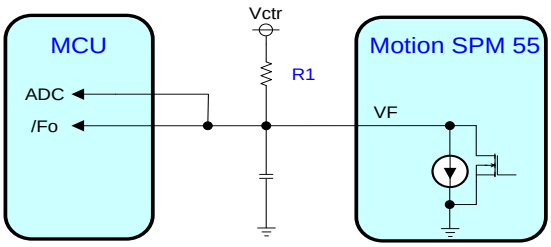


Figure 21. Proposed Circuit for Over-Temperature Protection

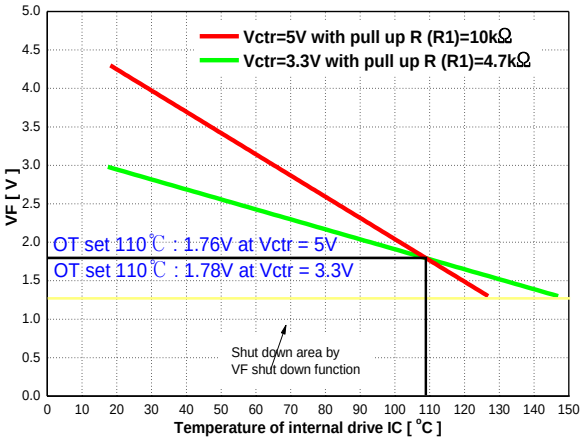


Figure 22. Voltage of VF Terminal according to internal drive IC temperature

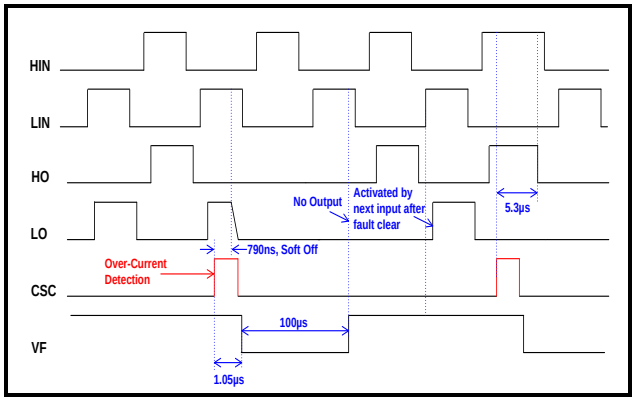


Figure 23. Fault-Out Function of VF Terminal

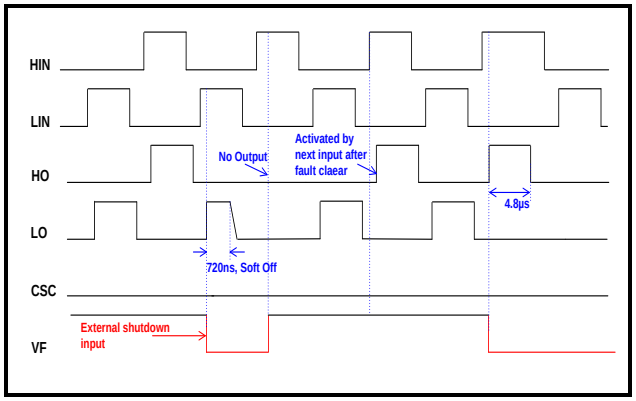


Figure 24. Shutdown Function of VF Terminal

5.5 Circuit of Input Signal (IN(xH), IN(xL))

Figure 25 shows the I/O interface circuit between the MCU and Motion SPM 55. Because the Motion SPM 55 input logic is active HIGH and there are built-in pull-down resistors, external pull-down resistors are not needed.

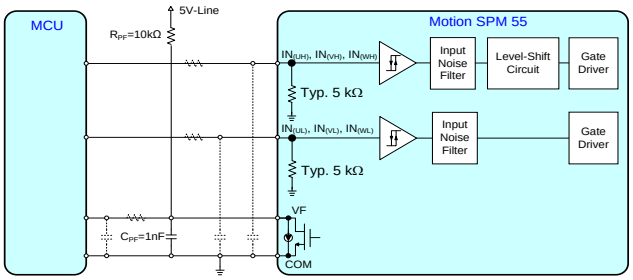


Figure 25. Recommended CPU I/O Interface Circuit

The input and fault output maximum rated voltages are shown in Table 16. Since the fault output is open drain, its rating is V_{DD} +0.3 V, 15 V supply interface is possible. However, it is recommended that the fault output be configured with the 5 V logic supplies, which is the same as the input signals. It is also recommended that the de-coupling capacitors be placed at both the MCU and Motion.

SPM 55 ends of the signal line for VF pin, as close as possible to each device. The RC coupling at each input (parts shown dotted in Figure 25) can be changed depending on the PWM control scheme used in the application and the wiring impedance of the PCB layout.

The input signal section of the Motion SPM 55 series integrates a 5 kΩ (typical) pull-down resistor. Therefore, when using an external filtering resistor between the MCU output and the Motion SPM 55 input, attention should be given to the signal voltage drop at the Motion SPM 55 input terminals to satisfy the turn-on threshold voltage requirement. For instance, R=100 Ω and C=1 nF for the parts shown dotted in Figure 25.

Table 16. Maximum Ratings of Input and VF Pins

Symbol	Item	Condition	Rating	Unit
V_{IN}	Input Signal Voltage	Applied between $IN_{(xH)}$, $IN_{(xL)}$-COM	-0.3 ~ V_{DD} +0.3	V
V_F	Fault Supply Voltage	Applied between VF-COM	-0.3 ~ V_{DD} +0.3	V

Table 17. Input Threshold Voltage Ratings (V_{DD}=15 V, T_J=25°C)

Symbol	Item	Condition	Min.	Max.	Unit
$V_{IN(ON)}$	Turn-On Threshold Voltage	$IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$-COM		2.4	V
$V_{IN(OFF)}$	Turn-Off Threshold Voltage	$IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$-COM	0.8		V

5.6 Bootstrap Circuit Design

5.6.1 Operation of Bootstrap Circuit

The V_{BS} voltage, which is the voltage difference between V_B (U, V, W) and V_S (U, V, W), provides the supply to the HVIC within the Motion SPM 55 series. This supply must be in the range of 13.0 V~18.5 V to ensure that the HVIC can fully drive the high-side IGBT. The under-voltage lockout protection for V_{BS} ensures that the HVIC does not drive the high-side IGBT if the V_{BS} voltage drops below a specific voltage (*refer to the datasheet of SPM55 series*). This function prevents the IGBT from operating in a high-dissipation mode.

There are a number of ways in which the V_{BS} floating supply can be generated. One of them is the bootstrap method described here (refer to Figure 26). This method has the advantage of being simple and inexpensive. However, the duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. The bootstrap supply is formed by a combination of a bootstrap diode, resistor, and The current flow path of the bootstrap circuit is shown in Figure 26. When V_S is pulled down to ground (low-side IGBT turn-on or low-side FRD freewheeling), the bootstrap capacitor (C_{BS}) is charged through the bootstrap diode (D_{BS}) and the resistor (R_{BS}) from the V_{DD} supply.

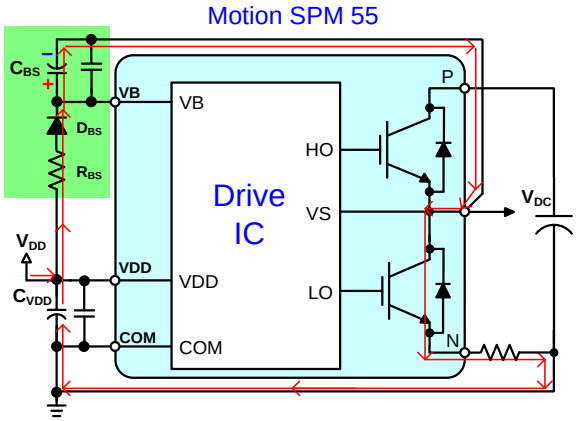


Figure 26. Current Path of Bootstrap Circuit for the Supply Voltage (VBS) of a HVIC when Low-Side IGBT Turns On

5.6.2 Selection of Bootstrap Capacitor Considering Initial Charging

Adequate on-time of the low-side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated by:

$$t_{charge} = C_{BS} \times R_{BS} \times \frac{1}{\delta} \times \ln \frac{V_{DD}}{V_{DD}-V_{BS(min)}-V_F-V_{LS}} \qquad (1)$$

where:

V_F = Forward voltage drop across the bootstrap diode;

$V_{BS(min)}$ =The minimum value of the bootstrap capacitor;

V_{LS} = Voltage drop across the low-side IGBT or load; and

δ = Duty ratio of PWM.

When the bootstrap capacitor is charged initially; V_{DD} drop voltage is generated based on initial charging method, V_{DD} line SMPS output current, V_{DD} source capacitance, and bootstrap capacitance. If VDD drop voltage reaches UV_{DDD} level, the low side is shutdown and a fault signal is activated. To avoid this malfunction, related parameter and initial charging method should be considered. To reduce V_{DD} voltage drop at initial charging, a large V_{DD} source capacitor and selection of optimized low-side turn-on method are recommended. Adequate on-time duration of the low-side IGBT to fully charge the bootstrap capacitor is initially required before normal operation of PWM starts.

Figure 27 shows an example of initial bootstrap charging sequence. Once V_{DD} is established, V_{BS} needs to be charged by turning on the low-side IGBTs. PWM signals are typically generated by an interrupt triggered by a timer with a fixed interval, based on the switching carrier frequency. Therefore, it is desired to maintain this structure without creating complementary high-side PWM signals. The capacitance of V_{DD} should be sufficient to supply necessary charge to V_{BS} capacitance in all three phases. If a normal PWM operation starts before V_{BS} reaches V_{UVLO} reset level, the high-side IGBTs cannot switch without creating a fault signal. It may lead to a failure of motor start in some applications. If three phases are charged synchronously, initial charging current through a single shunt resistor may exceed the over-current protection level. Therefore, initial charging time for bootstrap capacitors should be separated, as shown in Figure 28. The effect of the bootstrap capacitance factor and charging method (low-side IGBT driving method) is shown in Figure 29.

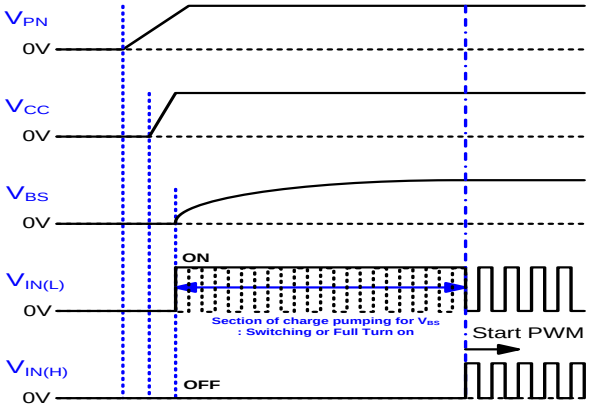


Figure 27. Timing Chart of Initial Bootstrap Charging

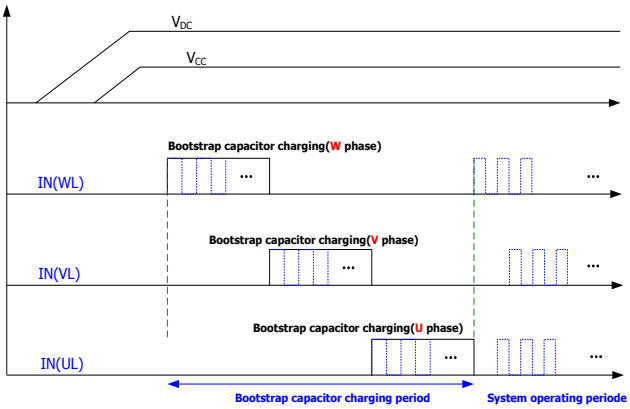


Figure 28. Recommended Initial Bootstrap Capacitors Charging Sequence

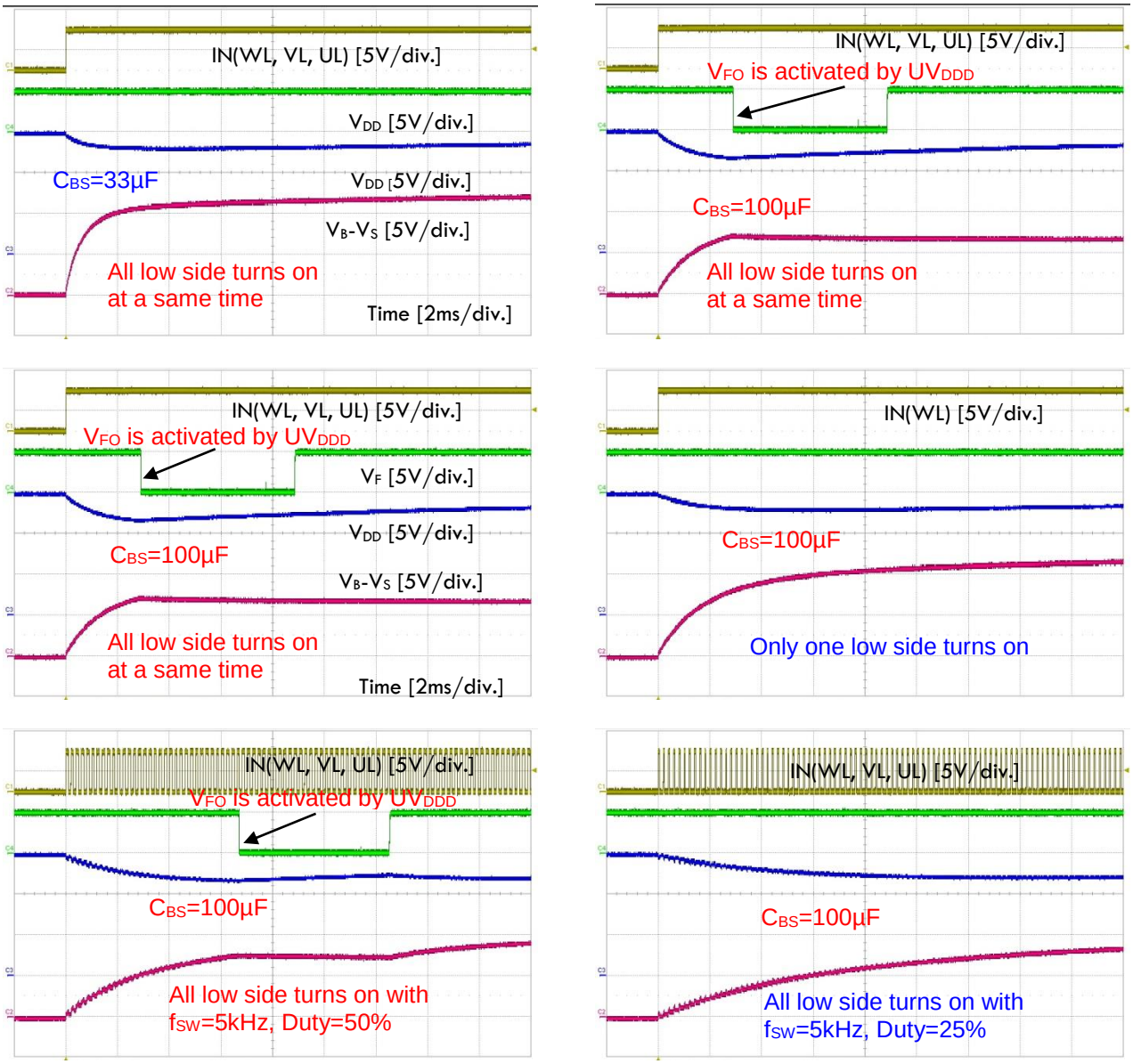


Figure 29.Initial Charging According to Bootstrap Capacitance and Charging Method (Ref. Condition: V_{DD}=15 V/300 mA, V_{DD} Capacitor=220 µF, Bootstrap Capacitor=100 µF, R_{BS}=20 Ω)

5.6.3 Selection of Bootstrap Capacitor Considering Operating

The bootstrap capacitance can be calculated by:

$$C_{BS} = \frac{I_{leak} \times \Delta t}{\Delta V_{BS}} \quad (2)$$

where:
Δt: maximum on pulse width of high-side IGBT;
ΔV_{BS}: the allowable discharge voltage of the C_{BS} (voltage ripple); and
I_{Leak}: maximum discharge current of the C_{BS}.

Mainly via the following mechanisms:

- Gate charge for turning the high-side IGBT on
- Quiescent current to the high-side circuit in HVIC
- Level-shift charge required by level-shifters in HVIC
- Leakage current in the bootstrap diode
- C_{BS} capacitor leakage current (ignored for non-electrolytic capacitors)
- Bootstrap diode reverse recovery charge

Practically, 2 mA of I_{Leak} is recommended for the Motion SPM 55 series. By considering dispersion and reliability, the capacitance is generally selected to be 2~3 times the calculated one. The C_{BS} is only charged when the high-side IGBT is off and the $V_{S(U,V,W)}$ voltage is pulled down to ground.

The on-time of the low-side IGBT must be sufficient to for the charge drawn from the C_{BS} capacitor to be fully replenished. This creates an inherent minimum on-time of the low-side IGBT (or off-time of the high-side IGBT).

Calculation Examples of Bootstrap Capacitance A;

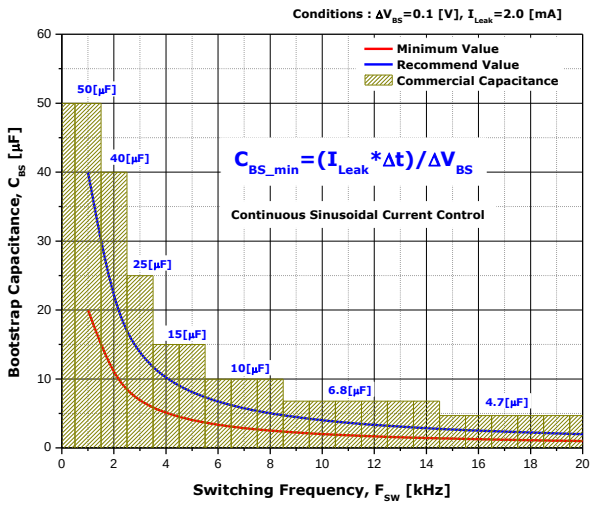


Figure 30. Capacitance of Bootstrap Capacitor on Variation of Switching Frequency

Based on switching frequency and recommended ΔV_{BS}

- I_{Leak}: circuit current = 2.0 mA (recommended value)
- ΔV_{BS}: discharged voltage = 0.1 V (recommended value)
- Δt: maximum on pulse width of high-side IGBT = 0.2 ms (depends on application)

$$C_{BS\_min} = \frac{I_{leak} \times \Delta t}{\Delta V_{BS}} = \frac{2mA \times 0.2ms}{0.1V} = 4.0 \times 10^{-6}$$

→ More than 2 times → 8 μF. (3)

Note:
40. The capacitance value can be changed according to the switching frequency, the capacitor selected, and the recommended V_{BS} voltage of 13.0~18.5 V (from datasheet). The above result is just a calculation example. This value can be changed according to the actual control method and lifetime of the component.

Calculation Examples of Bootstrap Capacitance B;

Based on operating conditions, UV_{BS} function, and allowable recommended $V_{B(X)}$-$V_{S(X)}$

To avoid unexpected under-voltage protection and to keep V_{BS} within recommended value, bootstrap capacitance should be selected based on the operating conditions. Bootstrap voltage ripple is influenced by bootstrap resistor, load condition, output frequency, and switching frequency. Check the bootstrap voltage under the maximum load condition in the system. Figure 31 shows example of $V_{B(X)}$-$V_{S(X)}$ ripple voltage during operation.

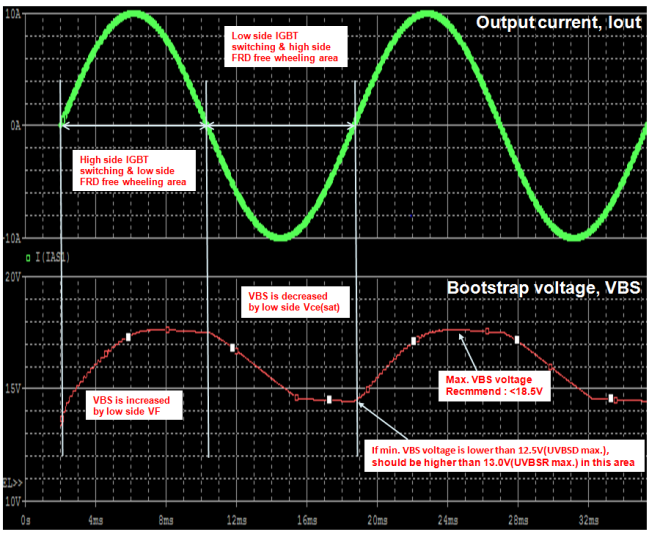


Figure 31. Recommendation of Bootstrap Ripple Voltage during Operation

5.6.4 Selection of Bootstrap Diode

When high side MOSFET or diode conducts, the bootstrap diode (D_{BS}) supports the entire bus voltage. Hence the withstand voltage more than 600 V is recommended. It is important that this diode should be fast recovery (recovery time < 100 ns) device to minimize the amount of charge that is fed back from the bootstrap capacitor into the V_{DD} supply. Similarly, the high voltage reverse leakage current is important if the capacitor has to store a charge for long periods of time.

5.6.5 Selection of Bootstrap Resistor

A resistor RBS must be added in series with the bootstrap diode to slow down the dV_{BS}/dt and to limit inrush current at initial CBS charging. It also determines the time to charge the bootstrap capacitor. That is, if the minimum ON pulse width of low-side MOSFET or the minimum OFF pulse width of high-side MOSFET is t_O, the bootstrap capacitor has to be charged ΔV during this period. Therefore, the value of bootstrap resistance can be calculated by the following equation.

$$R_{BS} = \frac{(V_{DD} - V_{BS}) \times t_O}{C_{BS} \times \Delta V_{BS}} \quad (4)$$

For the selection of R_{BS}, pulse power rating should be considered for initial charging of bootstrap capacitor. To use a large bootstrap capacitor, high pulse power rating is required for the bootstrap resistor. An example of resistor pulse power rating is shown in Figure 32.

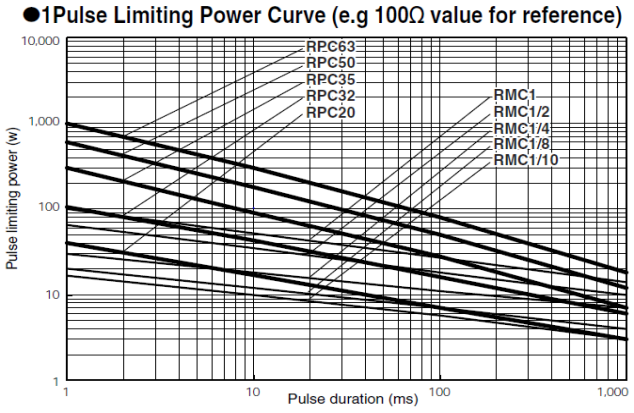


Figure 32. Example of Pulse Power Curve of Resistor (from KAMAYA OHM)

6 Print Circuit Board (PCB) Design

6.1 General Application Circuit Example

Figure 33 shows a general application circuitry of interface schematic with control signals connected directly to a MCU. Figure 34 shows guidance of PCB layout for Motion SPM 55.

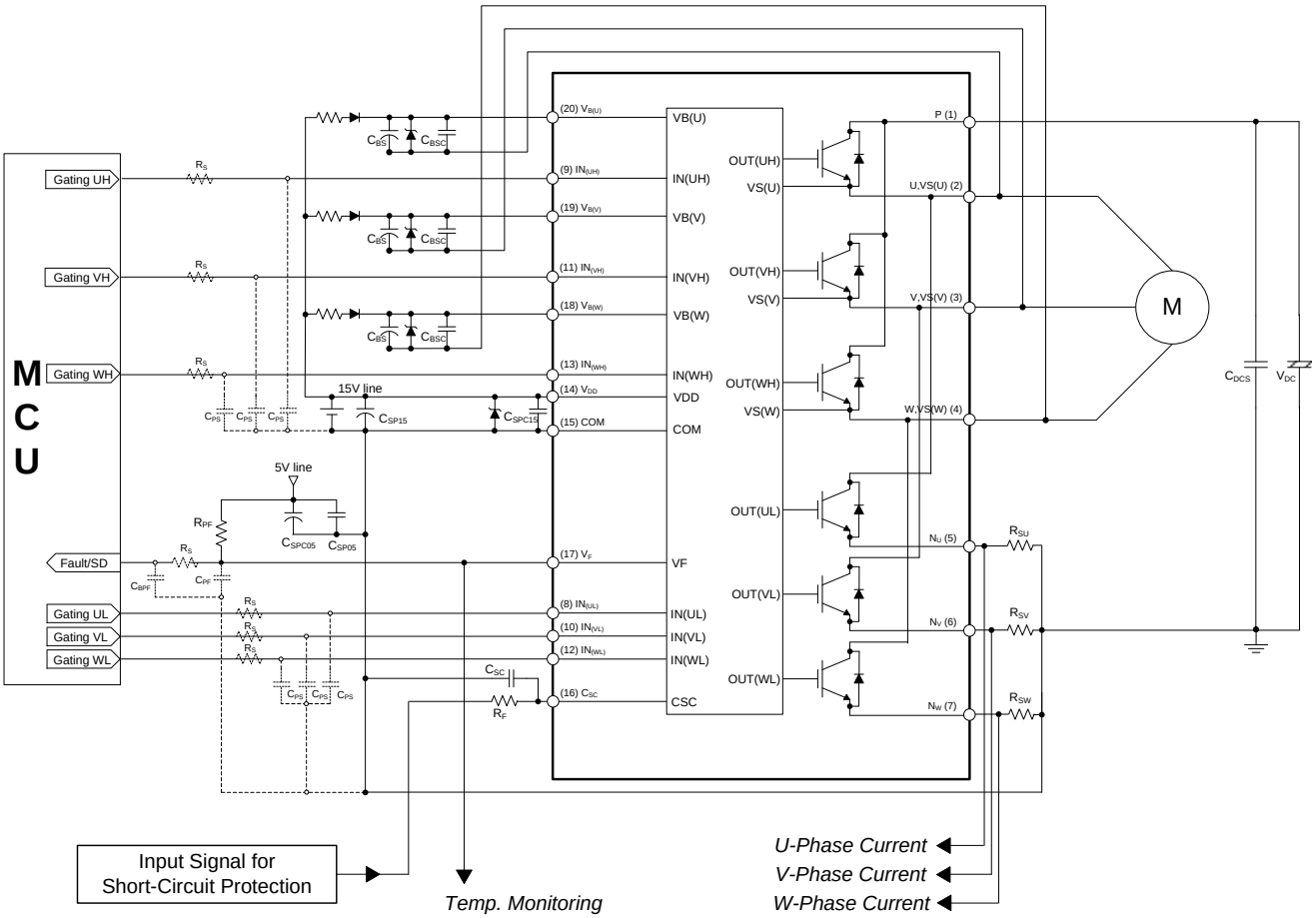


Figure 33. General Application Circuitry for Motion SPM 55

6.2 PCB Layout Guidance

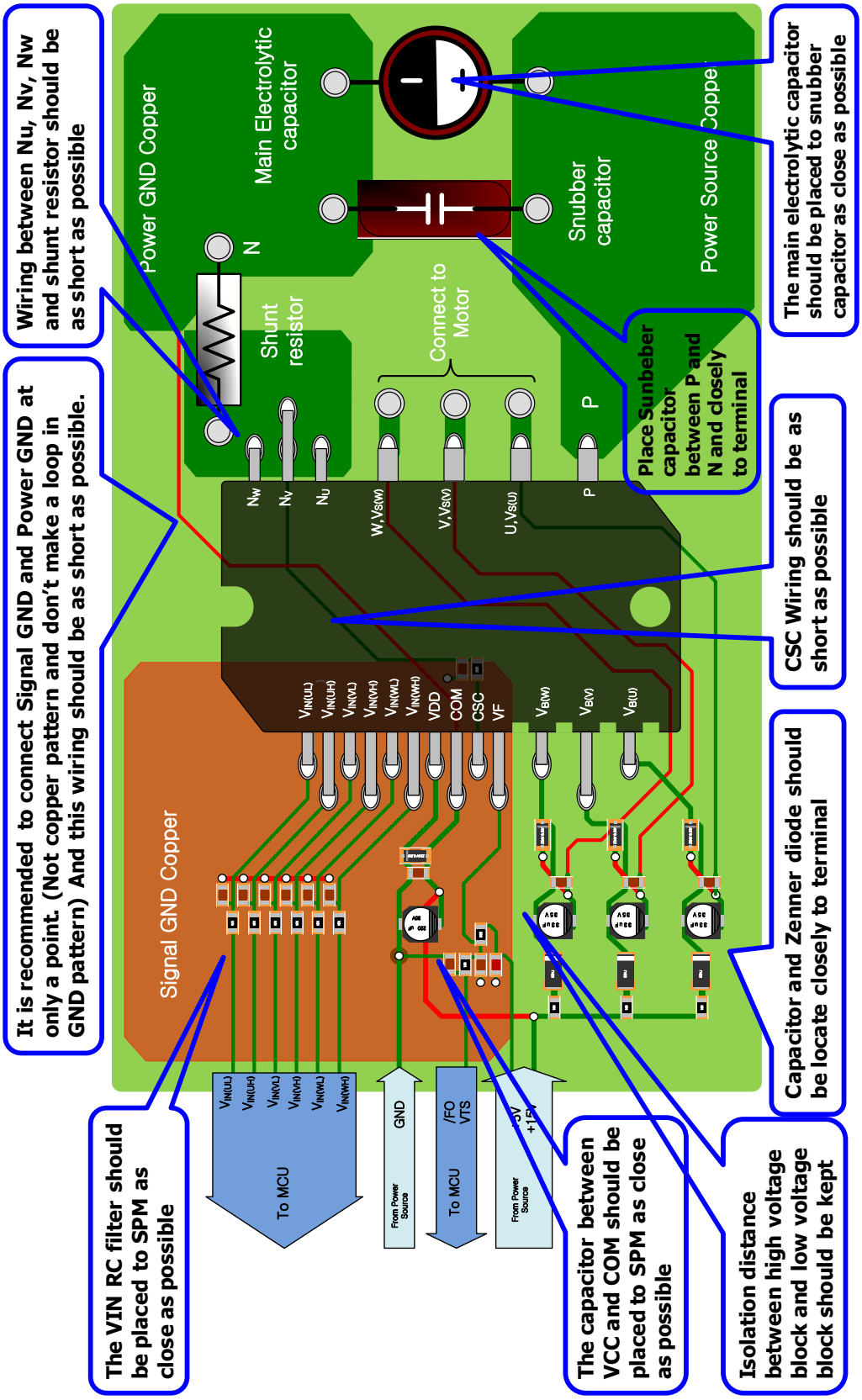
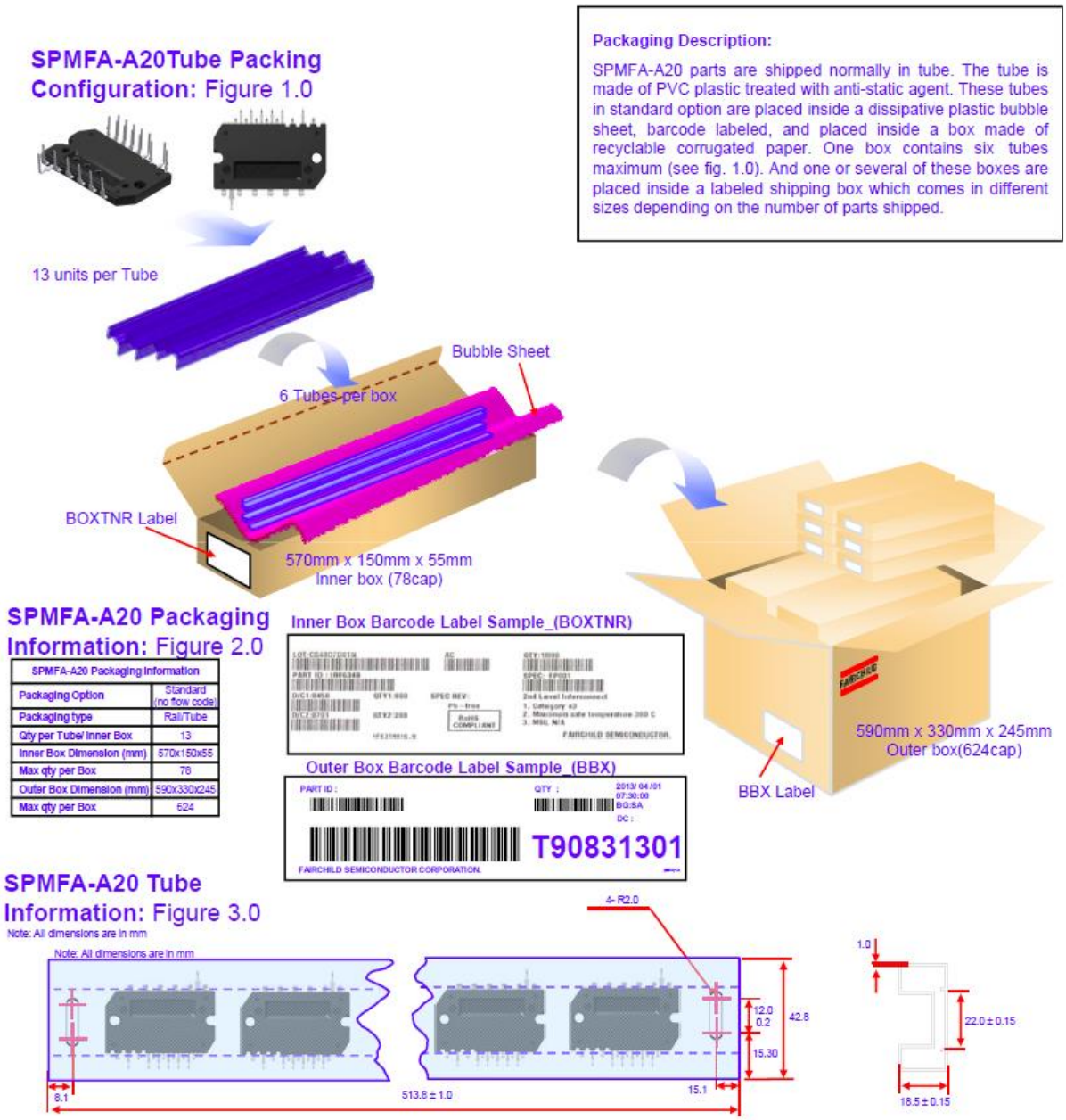


Figure 34. Print Circuit Board (PCB) Layout Guidance for Motion SPM 55

7 Packing Information



SPMFA-A20 Packaging Information	
Packaging Option	Standard (no flow code)
Packaging type	Rail/Tube
Qty per Tube/ Inner Box	13
Inner Box Dimension (mm)	570x150x55
Max qty per Box	78
Outer Box Dimension (mm)	590x330x245
Max qty per Box	624

Figure 35. Packing Information

8 Related Resources

FNB50560T1 Motion SPM® 55 Series

FNA51060T3 Motion SPM® 55 Series

FNB51060T1 Motion SPM® 55 Series

FNB51560T1 Motion SPM® 55 Series

FNA51560T3 Motion SPM® 55 Series

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