AN-1107
APPLICATION NOTE

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AC Signal Offset and Amplitude Control Using a Dual Channel Multiplying DAC and a Single I/V Converter

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INTRODUCTION

This application note describes how the circuit described herein removes the requirement for additional summing amplifiers and the IOUT architecture allows both ac and dc inputs, making this circuit ideal for data acquisition and instrumentation.

The circuit shown in Figure 1 consists of a large signal multiplying DAC, the AD5449, operating with an ac reference signal conditioned in Channel 1, and a +10 V input from an ADR01 in Channel 2, which shifts the offset of this signal.

The ADR01 is a low drift voltage reference with high accuracy and stability. Only one AD8065 is used to adjust the gain of the ac signal.

This is a good fit for this application with excellent ac performance and low noise, which makes the part ideal for this circuit's purpose. The DAC output currents are summed, and the voltage is converted by the AD8065. The ac signals, amplitude, and offset can then be controlled with a single DAC and an op amp.

FUNCTIONAL BLOCK DIAGRAM

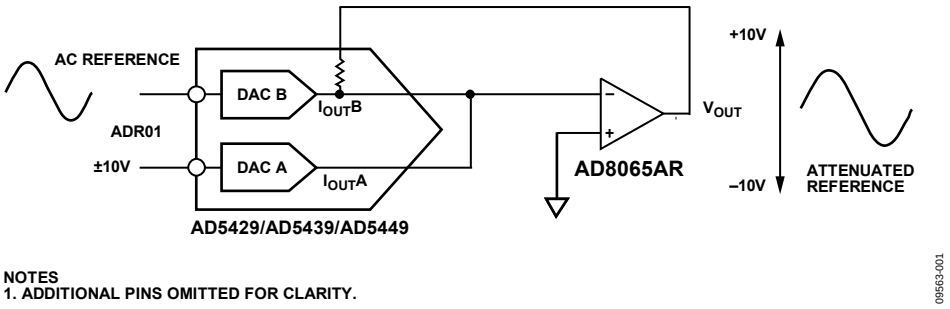

Figure 1.

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REVISION HISTORY

2/11—Revision 0: Initial Version

MULTIPLYING DACS

A multiplying DAC differs from the conventional fixed reference DAC in that it is able to operate with an arbitrary or ac reference signal.

A simple method of adjusting the gain of an ac signal is to use the classic inverter op amp stage, choose an amplifier with sufficient bandwidth, and adjust the gain by using the following equation:

$$V_{OUT} = -[RDAC/RFB\ (V_{IN})]$$

Multiplying DACs offer an ideal building block for multiplying an arbitrary or ac voltage signal. The buffered current output DAC architecture is based on a noninverting gain amplifier structure. A multiplying DAC uses an R-2R architecture to replicate the functionality of the variable RDAC resistor shown in Figure 2. The input impedance to the DAC seen at the V_{REF} pin is fixed, and the output impedance is code dependent to give the equivalent variable RDAC value.

In a multiplying DAC, as shown in Figure 3, current is steered to either the virtual ground connected to the $I_{OUT}1$ node or the ground node (in some parts, this is the $I_{OUT}2$ node), which allows for a very low glitch output voltage.

One of the key advantages in using an IOUT DAC in this configuration is that the integrated R_{FB} resistor is matched to the RDAC equivalent resistor, allowing for very low gain temperature coefficient errors.

When an output amplifier is connected in unipolar mode, the output voltage is given by

$$V_{OUT} = -\frac{D}{2^n} \times V_{REF}$$

where:
D is the fractional representation of the digital word loaded to the DAC.

D = 0 to 255 (8-bit DACs).

= 0 to 1023 (10-bit DACs).

= 0 to 4095 (12-bit DACs).

= 0 to 16,383 (14-bit DACs)

= 0 to 65,536 (16-bit DACs)

n is the number of bits.

In brief, the output signal of a multiplying DAC is proportional to the product of the reference input and the digital input number.

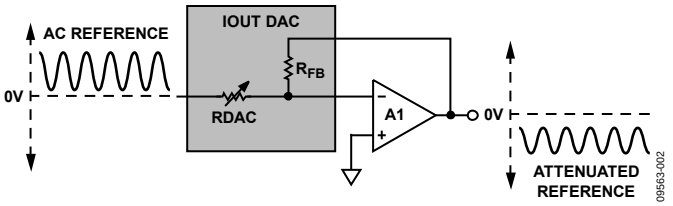

Figure 2. Inverting Gain Configuration

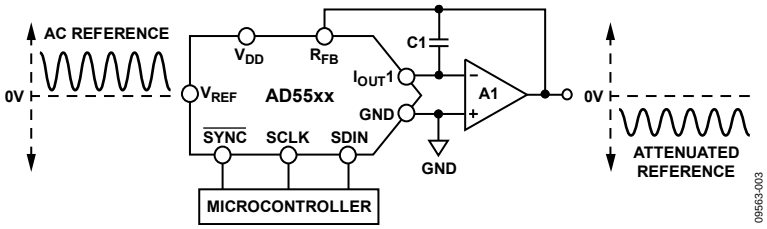

Figure 3. Multiplying DAC, V_{OUT} = 0 to $-V_{REF}$

ADDING GAIN

In applications in which the output voltage is required to be greater than V_{IN}, gain can be added with an additional external amplifier, or it can be achieved in a single stage.

Increase the gain of the circuit by using the recommended configuration shown in Figure 4. R1, R2, and R3 should have similar temperature coefficients, but they must not match the temperature coefficients of the DAC.

STABILITY ISSUES

An important component to take into account in achieving the desired waveform conditioning signal is the compensation capacitor. The internal output capacitance of the DAC introduces a pole into the open-loop response, which can cause ringing or instability in the closed-loop ramp profiling circuit. To compensate, an external feedback capacitor, C1 in Figure 3, is usually connected in parallel with the internal R_{FB} of the DAC.

If the value of C1 is too small, it can produce waveform distortion at the output, and if the value of C1 is too large, it can adversely affect the bandwidth of the system.

Because the internal output capacitance of the DAC varies with code, it is difficult to fix a precise value for C1. The value is best approximated according to the following equation:

$$C1 = 20\sqrt{\frac{C_O}{2\pi \times R_{FB}} \times \frac{1}{GBW}}$$

where:
GBW is the small signal unity gain bandwidth product of the op amp in use.
C_O is the output capacitance of the DAC.

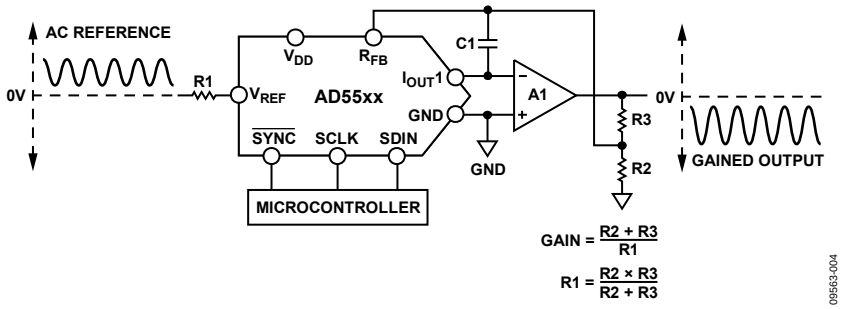

Figure 4. Signal Gain Using Multiplying DACs

OUTPUT VOLTAGE

Using a fixed 10 V reference in DAC A and a 4 V sinusoidal with a 2 V offset reference signal as the input in DAC B, the output voltage obtained in the AD5449 varies depending on the code and DAC loaded by

DAC A: change in the offset (0 V to 10 V)

DAC B: change in the amplitude (0 V to 4 V)

As the output voltage is connected in unipolar mode, the output voltage is given by

$$V_{OUT} = -V_{REF} \times D/2^n$$

where:
D is the fractional representation of the digital word loaded to the DAC; it can take a value from 0 to 4095.
n is the number of bits.

CODE LOADING EXAMPLES

Figure 5, Figure 6, and Figure 7 show the output voltage when both DAC A and DAC B are loaded with a digital code.

The expected output offset is the sum of the voltage in DAC A and the offset voltage in DAC B, being the output signal inverted by the op amp.

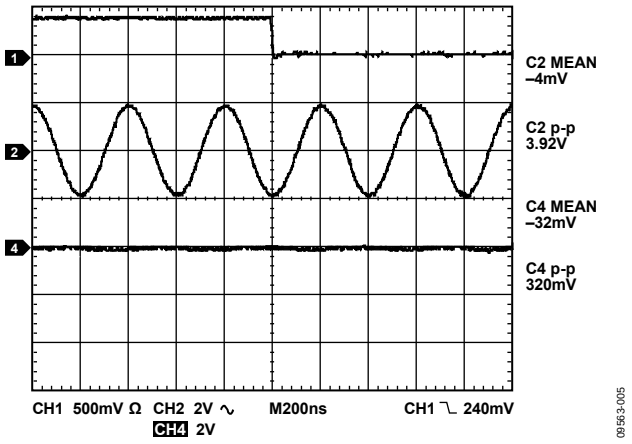

Figure 5. Zero Scale

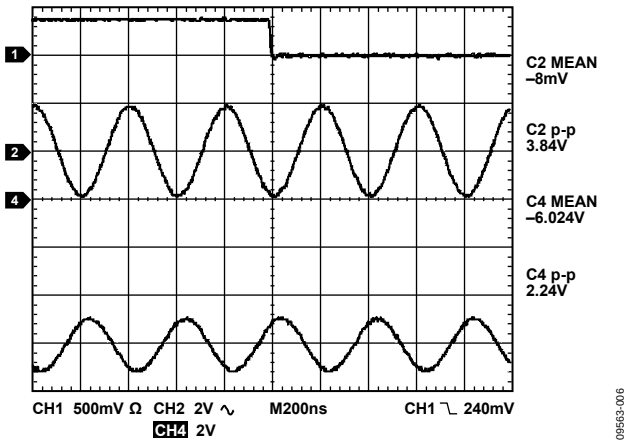

Figure 6. Half Scale

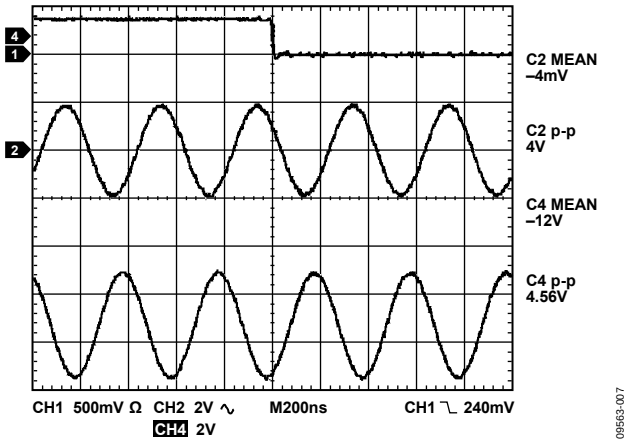

Figure 7. Full Scale

CHOOSING THE CORRECT OP AMP.

The performance of a multiplying DAC solution is strongly dependent on the selected op amp to perform the current to voltage conversion. In order to maintain the dc accuracy of the signal, it is important to select an operational amplifier with low bias current and low offset voltage so as not to swamp the minimum resolution of the DACs output. More detail on this is included in the appropriate multiplying DAC data sheets.

For applications where a relatively high speed ac or an arbitrary signal must be multiplied, a high bandwidth/high slew rate op amp is required to prevent the op amp from degrading the output signal. The gain bandwidth product of an op amp is limited by the feedback load realized with the feedback resistor. It is also limited by the gain configuration used to set up the part. To determine the gain bandwidth required, a general rule of thumb is to select an op amp with a −3 dB bandwidth of 10× the frequency of the signal to be conditioned.

The slew rate of the op amp is another specification that can limit the multiplying DAC if not carefully considered. As a rule of thumb for the AD54xx and AD55xx family of parts, an op amp with a slew rate of 100 V/µs is generally sufficient.

Table 1. Selection of Suitable Analog Devices High Speed Op Amps

Part No.	Supply Voltage (V)	BW @ ACL (MHz)	Slew Rate (V/µs)	V_{OS} (Maximum) (µV)	I_B (Max) (nA)	Packages
AD8065	5 to 24	145	180	1500	0.006	SOIC-8, SOT-23-5
AD8066	5 to 24	145	180	1500	0.006	SOIC-8, MSOP-8
AD8021	5 to 24	490	120	1000	10,500	SOIC-8, MSOP-8
AD8039	3 to 12	350	425	3000	750	SOIC-8, SC70-5, SOT-23-5
ADA4899	5 to 12	600	310	35	100	LFCSP-8, SOIC-8
AD8057	3 to 12	325	850	5000	500	SOT-23-5, SOIC-8
AD8058	3 to 12	325	850	5000	500	SOIC-8, MSOP-8
AD8061	2.7 to 8	320	650	6000	350	SOT-23-5, SOIC-8
AD8062	2.7 to 8	320	650	6000	350	SOIC-8, MSOP-8
AD9631	±3 to ±6	320	1300	10,000	7000	SOIC-8, PDIP-8

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