

150 W Eighth Brick Module for the [ADP1050](#), Digital Controller for Isolated Power Supply with PMBus Interface

FEATURES

- Standard eighth brick size (DOSA compatible)
- Full digital control
- Active clamp forward topology
- Input voltage range: 36 V dc to 75 V dc
- Output voltage: 6 V dc
- Maximum output current: 25 A
- Efficiency: typical 94% at full load
- PMBus™ communication
- Software graphical user interface (GUI)

APPLICATIONS

- 48 V telecom dc-to-dc power supply
- Telecommunications systems

GENERAL DESCRIPTION

This [ADP1050-ACF-150EB](#) is an eighth brick power module designed with the [ADP1050](#), a digital controller for isolated power supply with an PMBus interface.

With the excellent performance of the [ADP1050](#), this brick module achieves high efficiency, high integration, and low cost. Figure 4 shows the block diagram of this brick module. The high integration feature helps to reduce external components as much as possible. It also helps to achieve a low cost design.

MODULE PHOTOGRAPHS

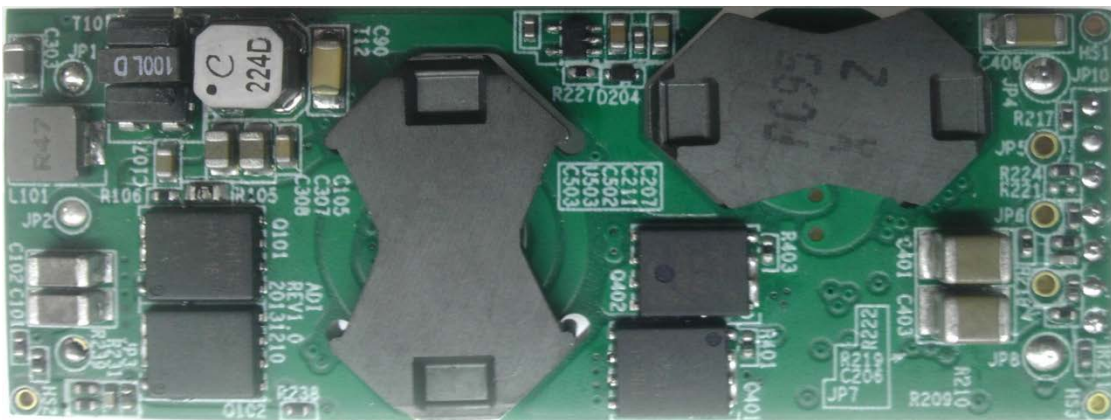


Figure 1. Top View

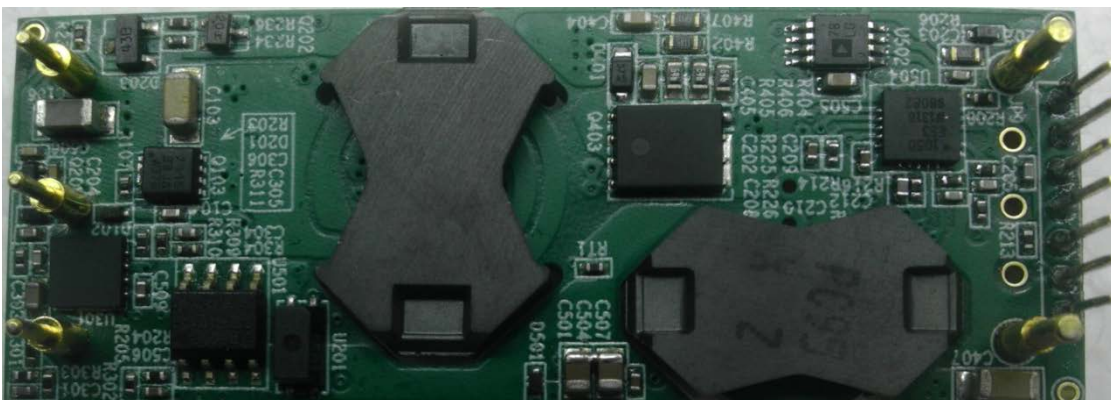


Figure 2. Bottom View

TABLE OF CONTENTS

Features	1	Test Setup.....	5
Applications.....	1	Test Equipment.....	5
General Description	1	Test Procedure	5
Module Photographs	1	Standard DC-to-DC Test Report	7
Revision History	2	Schematics and Artwork	29
Terminals	3	Ordering Information.....	35
Power Module Specifications	4	Bill of Materials.....	35

REVISION HISTORY

10/14—Revision 0: Initial Version

TERMINALS

Table 1. List of Terminals

Terminal	Name	Function
JP1	VIN+	Positive terminal of input power.
JP2	ON/OFF	Control pin of the 1/8 brick. Negative logic.
JP3	VIN-	Negative terminal of input power.
JP4	VOUT+	Positive terminal of output power.
JP5	VSENSE+	Positive sensing point.
JP6	NC	Not connected.
JP7	VSENSE-	Negative sensing point. Connected to VOUT-.
JP8	VOUT-	Negative terminal of output power.
JP10.1	SYNC/FLAGI	External flag input or frequency synchronous input.
JP10.2	AGND	Ground for control circuit.
JP10.3	SDA	Data bus of the PMBus interface.
JP10.4	PG	Power-good signal pin.
JP10.5	SCL	Clock bus of the PMBus interface.
JP10.6	6V	Auxiliary power on secondary side.
JP10.7	ADD	Address selection pin. Follow the specification listed in the ADP1050 data sheet.

POWER MODULE SPECIFICATIONS

Table 2. Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comment
Input Voltage	V_{IN}	36	48	75	V	
Turn-On Input Voltage	V_{INON}		34		V	
Turn-Off Input Voltage	V_{INOFF}		32		V	
Maximum Input Current	I_{INMAX}			5	A	
No Load Input Current	$I_{IN,No Load}$		50		mA	$V_{IN} = 48 V$
Standby Input Current	$I_{IN,Standby}$		10		mA	$V_{IN} = 48 V$
Output Voltage	V_{OUT}		6		V	
OVP			6.94		V	
Output Voltage Ripple			70	100	mV	
Output Current	I_{OUT}			25	A	
OCP			32		A	
Efficiency	η		94		%	Airflow = 200 LFM or above
Switching Frequency	f_{sw}		297.5		kHz	$V_{IN} = 48 V, I_{OUT} = 25 A$
External Capacitance		470			μF	
Dynamic Load Response						
Peak Deviation	V_{PK}		3		$\% \times V_{OUT}$	
Settling Time	t_S		200		μs	

TEST SETUP

TEST EQUIPMENT

- DC voltage source: adjustable dc source that is capable of outputting 36 V dc to 75 V dc, with a minimum power rating of 150 W.
- DC multimeter: a four digits multimeter that is capable of handling 0 V dc to 80 V dc or greater. Moreover, a four digits multimeter that is capable of handling 0 V dc to 7 V dc or greater.
- Output load: dc load that is capable of receiving 0 V dc to 7 V dc, 0 A to 25 A, and 0 W to 150 W or greater.
- Oscilloscope: 500 MHz full bandwidth is recommended.
- Fan: 200 LFM forced air-cooling.

TEST PROCEDURE

To conduct the test procedure power up and shut down the module.

To power up the module, use the following steps:

1. Connect the input terminals (JP1, JP3) to the input source, and connect the output terminals (JP4, JP8) to the load.

2. Place a resistor between the ADD pin (JP10.15) and the AGND pin (JP10.10). Select the resistance based on the information given in the [ADP1050](#) data sheet.
3. (Optional.) Add a pull-up resistor (2.2 k Ω typical) between the PG pin (JP10.12) and an external dc source. The dc voltage of this dc source must not exceed 3.6 V.
4. (Optional.) Connect the SDA pin (JP10.11), SCL pin (JP10.13), and the AGND pin (JP10.10) to the PMBus interface if communication from the PMBus interface to other PMBus devices is necessary.
5. Place an external aluminum capacitor of 470 μ F (or greater) between the output terminals (JP4, JP8).
6. Connect the ON/OFF pin (JP2) to ground for input power (JP3).
7. Apply a dc voltage source (36 V dc ~ 75 V dc) between the input terminals (JP1, JP3).

To shut down the module, use the following steps:

1. Shut down the input dc voltage source.
2. Shut down the load.

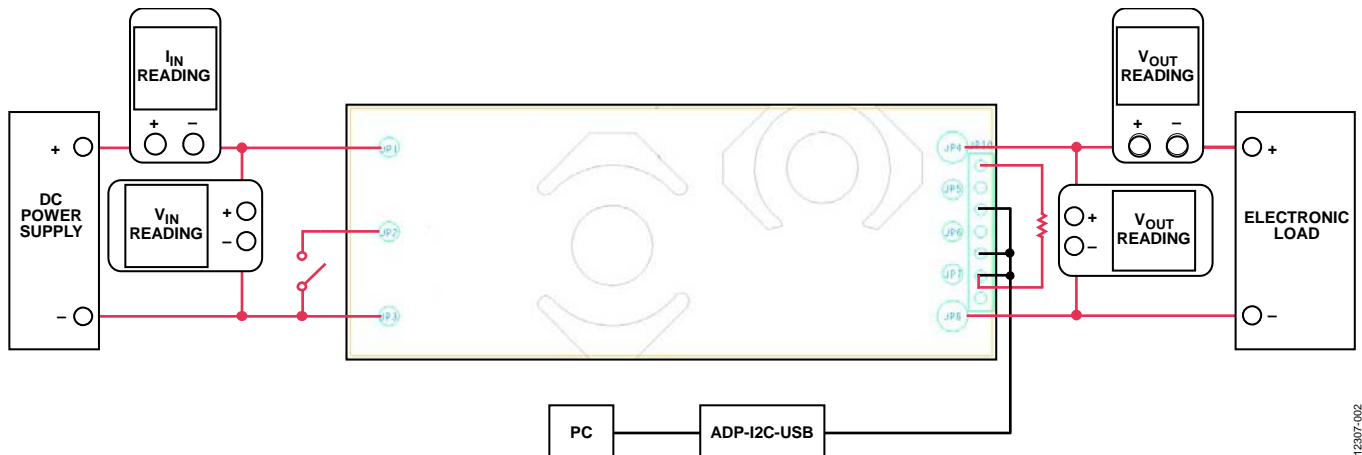


Figure 3. Test Configuration

12307-002

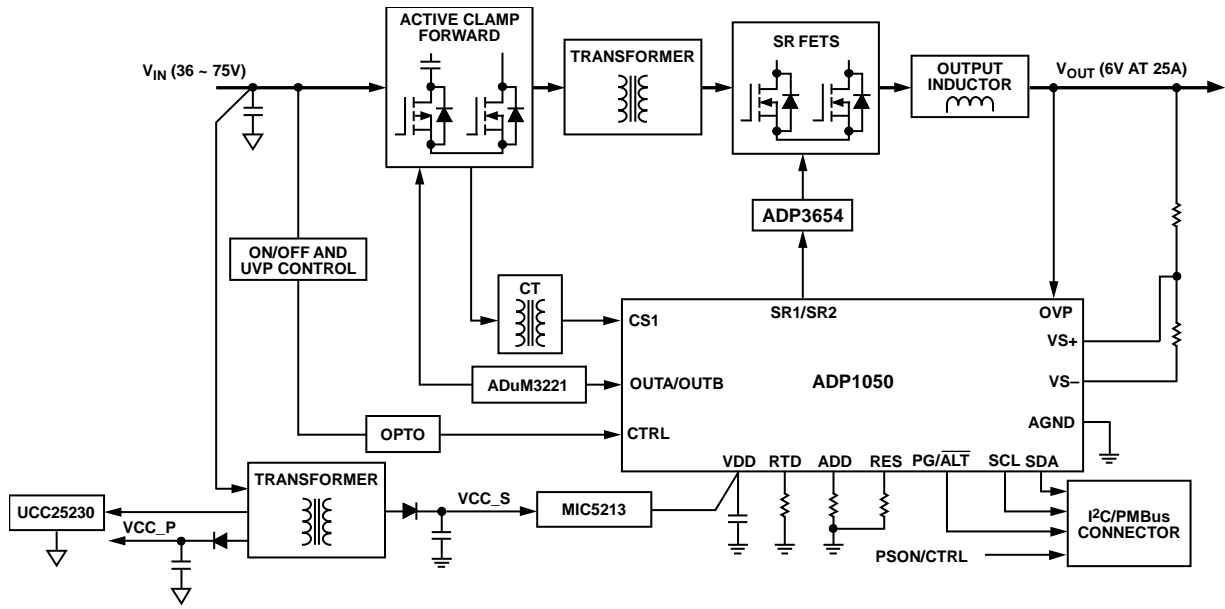


Figure 4.

12307-001

STANDARD DC-TO-DC TEST REPORT

Table 3. Test Summary

Item	Test	Specification	Result
Input Characterization			
1.1	Efficiency	$V_{IN} = 48\text{ V}$, $I_{OUT} = 25\text{ A}$; efficiency > 94.0% typ	Pass
1.2	Input undervoltage lockout	31 V ~ 33 V/33 V ~ 35 V	Pass
1.3	Maximum input current	5 A	Pass
1.4	No load input current	50 mA typ	Pass
1.5	Off converter input current	10 mA typ	Pass
Output Characterization			
2.1	Output voltage set point	6 V	Pass
2.2	Output voltage regulation	5.92 V ~ 6.08 V	Pass
2.3	Output ripple and noise	<100 mV p-p with 20 MHz bandwidth	Pass
2.4	Dynamic load response	Peak voltage deviation < 180 mV; settling time < 100 μ s	Pass
2.5	Turn-on transient	Overshoot < 5% V_{OSET}	Pass
2.6	Turn-off transient	No specification	Pass
2.7	Stability	See the 2.7 Stability section	Pass
2.8	Prebias Test	See the 2.8 Prebias Test section	Pass
Protection			
3.1	Overcurrent protection	No damage	Pass
3.2	Short-circuit protection	Hiccup mode (1 sec)	Pass
3.3	Overvoltage protection	<7.0 V	Pass

Input Characterization

1.1 Efficiency

Test conditions:

- The unit is set at maximum load, and the input voltage is varied from the minimum to the maximum value.
- Efficiency is measured after device warms up for at least 10 minutes.

Pass/fail criteria:

- $V_{IN} = 48\text{ V}$, $I_{OUT} = 25\text{ A}$, efficiency > 94.0%.

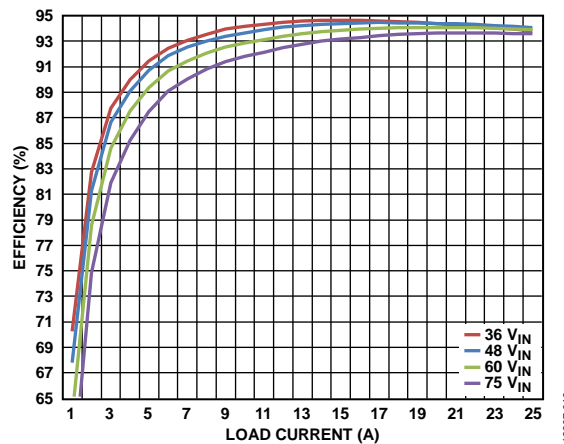


Figure 5. Efficiency Chart

Table 4. Efficiency Data

V _{IN} (V)	I _{IN} (A)	V _{OUT} (V)	I _{OUT} (A)	Efficiency (%)	V _{IN} (V)	I _{IN} (A)	V _{OUT} (V)	I _{OUT} (A)	Efficiency (%)
35.9970	0.0658	5.9870	0.0054	1.36	48.0040	0.0535	5.9870	0.0054	1.26
35.9820	0.2189	5.9870	0.9239	70.23	47.9710	0.1702	5.9872	0.9244	67.79
35.9650	0.3870	5.9860	1.9243	82.76	47.9750	0.2957	5.9867	1.9258	81.27
35.9490	0.5670	5.9856	2.9879	87.74	47.9650	0.4306	5.9862	2.9894	86.64
35.9330	0.7261	5.9851	3.9227	89.98	47.9540	0.5496	5.9860	3.9241	89.13
35.9170	0.8960	5.9847	4.9167	91.43	47.9470	0.6770	5.9851	4.9191	90.70
35.8830	1.0788	5.9840	5.9798	92.44	47.9350	0.8131	5.9850	5.9827	91.87
35.8790	1.2384	5.9835	6.9121	93.08	47.9260	0.9331	5.9838	6.9160	92.54
35.8640	1.4103	5.9830	7.9095	93.56	47.9120	1.0621	5.9832	7.9120	93.03
35.8460	1.5940	5.9819	8.9741	93.95	47.9040	1.2001	5.9832	8.9761	93.42
35.8390	1.7550	5.9816	9.9015	94.16	47.8940	1.3209	5.9826	9.9054	93.67
35.8190	1.9290	5.9810	10.8980	94.34	47.8830	1.4503	5.9810	10.9029	93.90
35.8030	2.1143	5.9798	11.9601	94.48	47.8670	1.5886	5.9803	11.9660	94.11
35.7840	2.2771	5.9788	12.8914	94.59	47.8580	1.7098	5.9793	12.8933	94.21
35.7300	2.4667	5.9773	13.9535	94.63	47.8500	1.8487	5.9783	13.9555	94.31
35.7560	2.6405	5.9763	14.9529	94.65	47.8390	1.9801	5.9771	14.9554	94.37
35.7430	2.8057	5.9755	15.8808	94.63	47.8260	2.1020	5.9761	15.8847	94.43
35.7350	2.9950	5.9740	16.9454	94.59	47.8150	2.2425	5.9756	16.9493	94.46
35.7350	3.1715	5.9729	17.9399	94.55	47.7920	2.3745	5.9730	17.9419	94.43
35.7050	3.3412	5.9717	18.8731	94.47	47.7830	2.4982	5.9721	18.8756	94.43
35.6880	3.5334	5.9694	19.9387	94.39	47.7720	2.6398	5.9704	19.9402	94.40
35.6730	3.7151	5.9678	20.9342	94.27	47.7610	2.7733	5.9690	20.9372	94.35
35.6590	3.8841	5.9664	21.8650	94.19	47.7520	2.8978	5.9675	21.8660	94.30
35.6490	4.0790	5.9650	22.9286	94.06	47.7410	3.0405	5.9652	22.9281	94.22
35.6340	4.2631	5.9640	23.9295	93.95	47.7290	3.1753	5.9639	23.9266	94.16
35.6490	4.4313	5.9613	24.8588	93.81	47.7220	3.3011	5.9618	24.8515	94.05
48.0040	0.0535	5.9870	0.0054	1.26	75.0060	0.0512	5.9864	0.0008	0.13
47.9710	0.1702	5.9872	0.9244	67.79	75.9990	0.1254	5.9857	0.9244	58.06
47.9750	0.2957	5.9867	1.9258	81.27	74.9930	0.2054	5.9854	1.9263	74.85
47.9650	0.4306	5.9862	2.9894	86.64	74.9850	0.2914	5.9849	2.9904	81.91
47.9540	0.5496	5.9860	3.9241	89.13	74.9790	0.3674	5.9840	3.9241	85.24
47.9470	0.6770	5.9851	4.9191	90.70	74.9730	0.4489	5.9837	4.9201	87.48
47.9350	0.8131	5.9850	5.9827	91.87	74.9630	0.5360	5.9831	5.9823	89.08
47.9260	0.9331	5.9838	6.9160	92.54	74.9530	0.6130	5.9828	6.9165	90.06
47.9120	1.0621	5.9832	7.9120	93.03	74.9460	0.6954	5.9820	7.9134	90.83
47.9040	1.2001	5.9832	8.9761	93.42	74.9370	0.7840	5.9807	8.9771	91.38
47.8940	1.3209	5.9826	9.9054	93.67	74.9300	0.8612	5.9804	9.9059	91.80
47.8830	1.4503	5.9810	10.9029	93.90	74.9250	0.9445	5.9790	10.9038	92.13
47.8670	1.5886	5.9803	11.9660	94.11	74.9190	1.0321	5.9781	11.9660	92.51
47.8580	1.7098	5.9793	12.8933	94.21	74.8890	1.1098	5.9772	12.8963	92.75
47.8500	1.8487	5.9783	13.9555	94.31	74.8820	1.1978	5.9766	13.9579	93.01
47.8390	1.9801	5.9771	14.9554	94.37	74.8890	1.2810	5.9758	14.9583	93.18
47.8260	2.1020	5.9761	15.8847	94.43	74.8840	1.3586	5.9746	15.8886	93.31
47.8150	2.2425	5.9756	16.9493	94.46	74.8750	1.4475	5.9725	16.9542	93.43
47.7920	2.3745	5.9730	17.9419	94.43	74.8550	1.5310	5.9719	17.9482	93.53
47.7830	2.4982	5.9721	18.8756	94.43	74.8700	1.6091	5.9709	18.8815	93.58
47.7720	2.6398	5.9704	19.9402	94.40	74.8700	1.6989	5.9701	19.9480	93.63
47.7610	2.7733	5.9690	20.9372	94.35	74.8600	1.7832	5.9681	20.9450	93.64
47.7520	2.8978	5.9675	21.8660	94.30	74.8580	1.8614	5.9662	21.8738	93.66
47.7410	3.0405	5.9652	22.9281	94.22	74.8460	1.9520	5.9650	22.9350	93.64
47.7290	3.1753	5.9639	23.9266	94.16	74.8410	2.0370	5.9630	23.9339	93.62
47.7220	3.3011	5.9618	24.8515	94.05	74.8320	2.1161	5.9613	24.8623	93.60

1.2 Input Undervoltage Lockout (Input UVP)

Test condition:

- The input voltage increases slowly from 30 V until the unit turns on.
- The input voltage decreases slowly from 36 V until the unit turns off.

Pass/fail criteria:

- The unit test shall meet the specification requirements.

Table 5. Input UVP

Parameter	Load (A)	Specification (V)			Test Results (V)		
		Min	Typ	Max	-40°C	+25°C	+85°C
Turn-On Voltage	0	33.0		35.0		34.1	
	25	33.0		35.0		34.1	
Turn-Off Voltage	0	31.0		33.0		32.6	
	25	31.0		33.0		32.6	
Pass or Fail						Pass	

1.3 Maximum Input Current

Test condition:

- The unit is set at maximum load, and the input voltage is set the minimum value.

Pass/fail criteria:

- The unit test shall meet the specification requirements.

Table 6. Maximum Input Current

V _{IN} (V)	Load (A)	Specification (A)			Test Results (A)		
		Min	Typ	Max	-40°C	+25°C	+85°C
33.3	25			5		4.736	
Pass or Fail						Pass	

1.4 No Load Input Current

Test condition:

- The unit is set at no load at the rated input voltage.

Pass/fail criteria:

- The unit test shall meet the specification requirements.

Table 7. No Load Input Current

V _{IN} (V)	Load (A)	Specification (mA)			Test Results (mA)		
		Min	Typ	Max	-40°C	+25°C	+85°C
36	0		50			65.8	
48	0		50			53.5	
75	0		50			51.2	
Pass or Fail						Pass	

1.5 Standby Input Current

Test condition:

- The unit is tested at the on/off pin grounded at the rated input voltage.

Pass/fail criteria:

- The unit test shall meet the specification requirements.

Table 8. Standby Input Current

V_{IN} (V)	Specification (mA)			Test Results (mA)		
	Min	Typ	Max	-40°C	+25°C	+85°C
36		10	12		10.1	
48		10	12		10.2	
75		10	12		11.5	
Pass or Fail					Pass	

Output Characterization**2.1 Output Voltage Set Point**

Test condition:

- The unit test shall meet the specification requirements.

Pass/fail criteria:

- The unit test shall meet the specification requirements.

Table 9. Output Voltage Set Point

V_{IN} (V)	Load (A)	Specification (V)			Test Results (V)		
		Min	Typ	Max	-40°C	+25°C	+85°C
48	25	5.92		6.08		5.9760	
Pass or Fail						Pass	

2.2 Output Voltage Regulation

Test condition:

- Test is repeated from different input voltages. The output is at minimum load then at maximum.

Pass/fail criteria:

- Regulation limit: $V_{OSET} \times (\pm 0.2\%)$

Table 10. Output Voltage Regulation

V_{IN} (V)	Load (A)	V_{OUT} (V)		
		-40°C	+25°C	+85°C
36	0		5.9934	
	25		5.9751	
48	0		5.9941	
	25		5.9760	
75	0		5.9913	
	25		5.9748	

Table 11. Line Regulation

V_{IN} (V)	Spec (mV)			Test Results (mV)		
	Min	Typ	Max	-40°C	+25°C	+85°C
36	-12		+12		9.15	
48	-12		+12		9.05	
75	-12		+12		8.25	
Pass or Fail					Pass	

Table 12. Load Regulation

Load V_{IN} (mV)	Spec (mV)			Test Results (mV)		
	Min	Typ	Max	-40°C	+25°C	+85°C
0	-12		+12		1.4	
25					0.6	
Pass or Fail					Pass	

2.3 Output Ripple and Noise

Test condition:

- See Figure 6 for test setup.

Pass/fail criteria:

- The unit test shall meet the specification requirements.

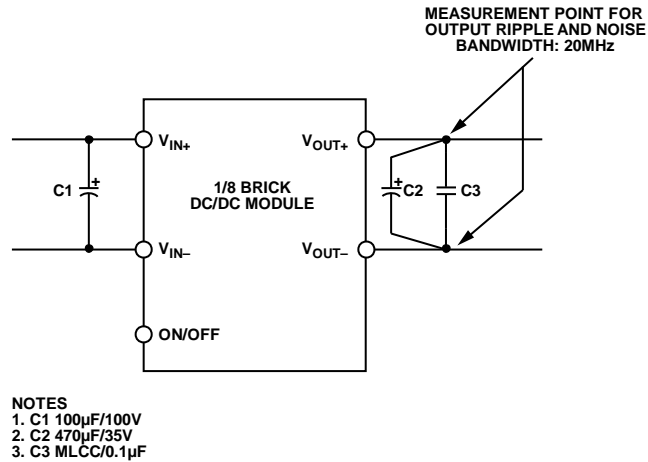


Figure 6. Ripple Test Configuration

Table 13. Ripple and Noise

Item	V _{IN} (V)	Load (A)	Specification (mV)			Test Results (mV)		
			Min	Typ	Max	-40°C	+25°C	+85°C
V p-p	36	0	0.000		100.000		56	
	48	0	0.000		100.000		78	
	75	0	0.000		100.000		86	
	36	25	0.000		100.000		54	
	48	25	0.000		100.000		74	
	75	25	0.000		100.000		92	
	Pass or Fail							Pass

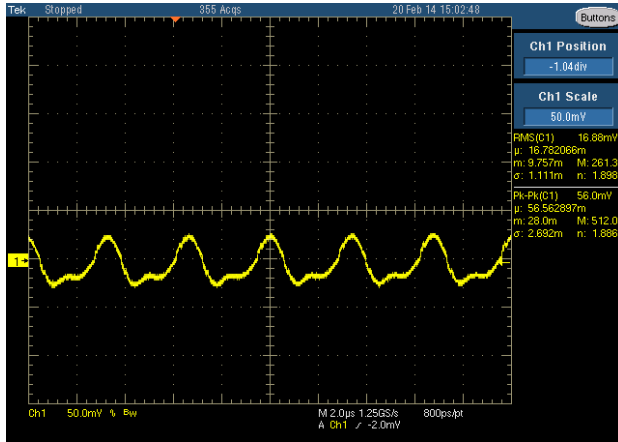


Figure 7. Ripple Waveform (CH1: Output Voltage) at 36 V_{IN}, 0 A at 25°C

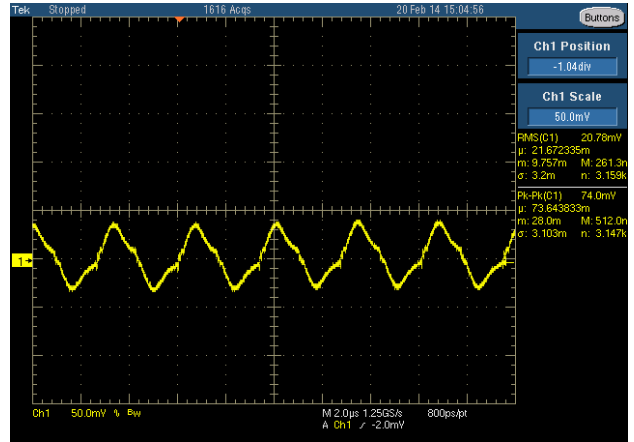


Figure 10. Ripple Waveform (CH1: Output Voltage) at 48 V_{IN}, 25 A at 25°C

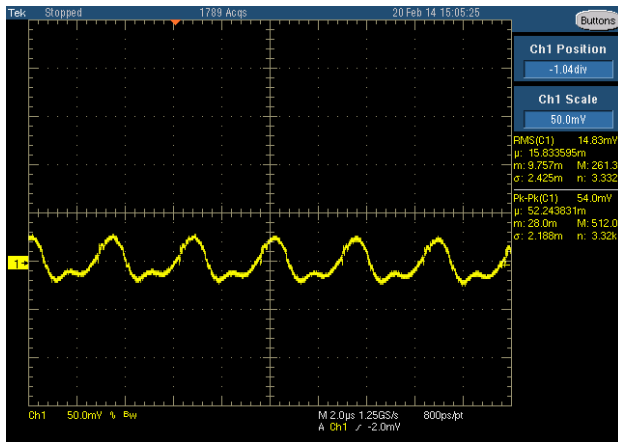


Figure 8. Ripple Waveform (CH1: Output Voltage) at 36 V_{IN}, 25 A at 25°C

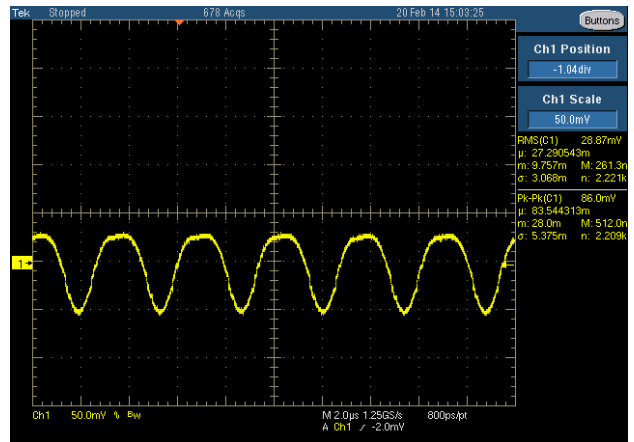


Figure 11. Ripple Waveform (CH1: Output Voltage) at 75 V_{IN}, 0 A at 25°C

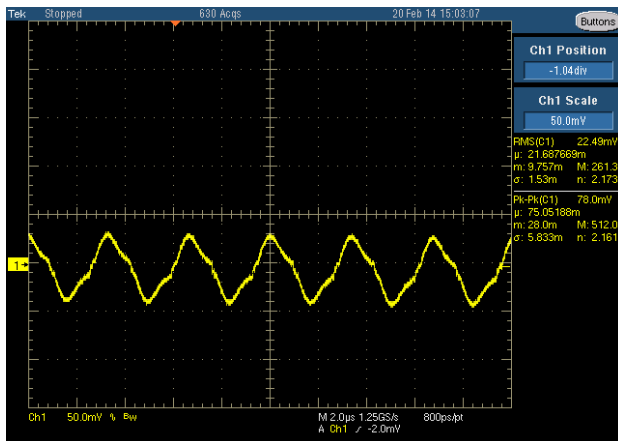


Figure 9. Ripple Waveform (CH1: Output Voltage) at 48 V_{IN}, 0 A at 25°C

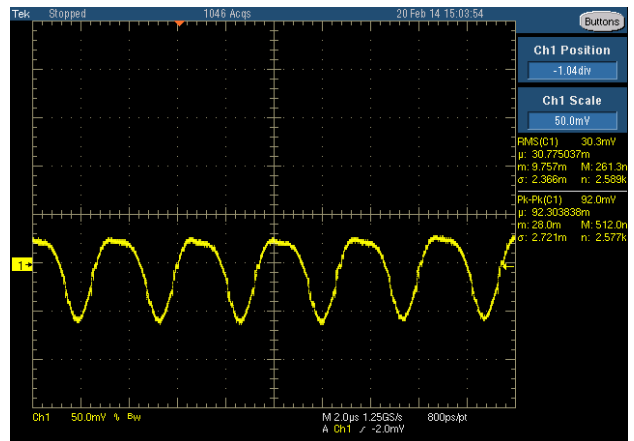


Figure 12. Ripple Waveform (CH1: Output Voltage) at 75 V_{IN}, 25 A at 25°C

2.4 Dynamic Load Response

Test condition:

- The dynamic load response changes at a rate and load step and frequency change are basis specification defined.

Pass/fail criteria:

- The unit test shall meet the specification requirements.

Table 14. Dynamic Load Transient Result¹

V _{IN} (V)	Load Step (%)	Specification (mV)			Test Results (mV)		
		Min	Typ	Max	-40°C	+25°C	+85°C
36	25% to 75%			180		144	
	75% to 25%			180		152	
48	25% to 75%			180		168	
	75% to 25%			180		160	
75	25% to 75%			180		168	
	75% to 25%			180		180	
Pass or Fail					Pass		

¹ Current slew rate = 0.1 A/μs, current step = 50%.

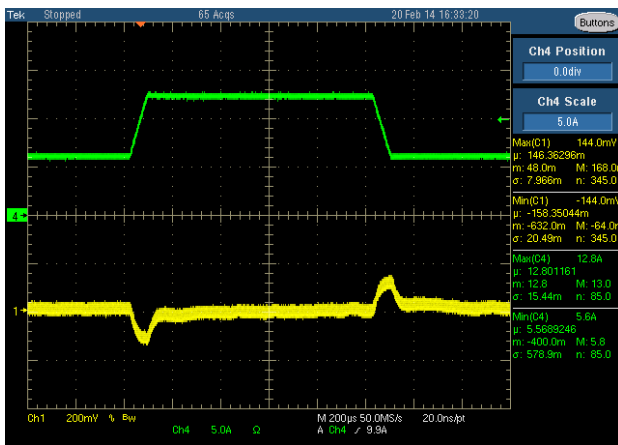


Figure 13. Dynamic Load Transient Waveform (CH1: Output Voltage; CH4: Output Current) at 36 V_{IN} at 25°C Load Step: 25% to 75%

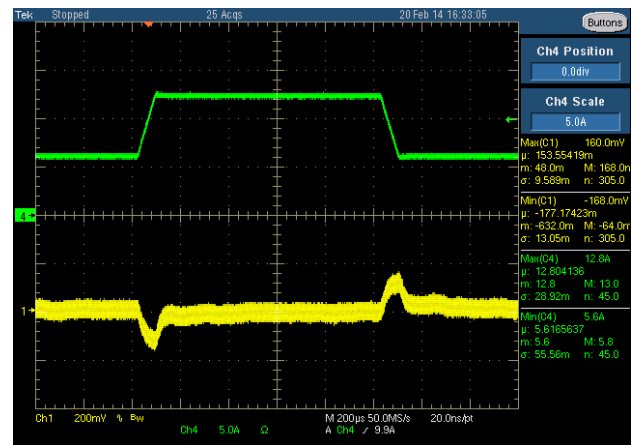


Figure 15. Dynamic Load Transient Waveform (CH1: Output Voltage; CH4: Output Current) at 48 V_{IN} at 25°C Load Step: 25% to 75%

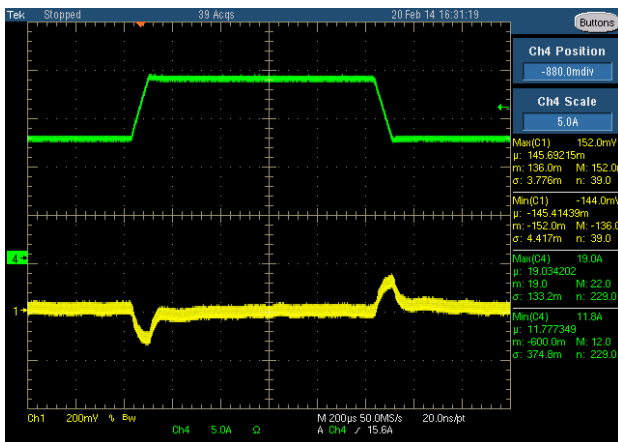


Figure 14. Dynamic Load Transient Waveform (CH1: Output Voltage; CH4: Output Current) at 36 V_{IN} at 25°C Load Step: 25% to 75%

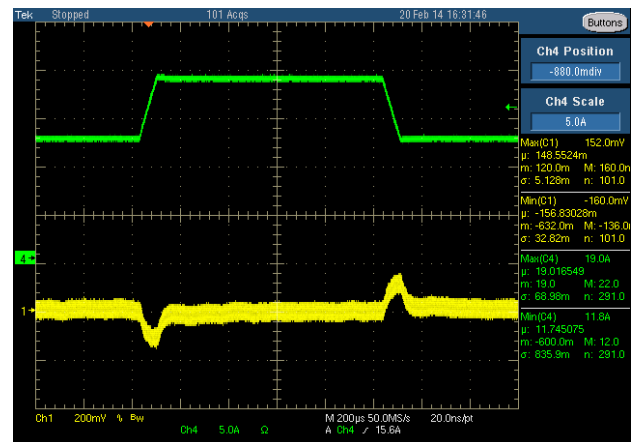


Figure 16. Dynamic Load Transient Waveform (CH1: Output Voltage; CH4: Output Current) at 48 V_{IN} at 25°C Load Step: 25% to 75%

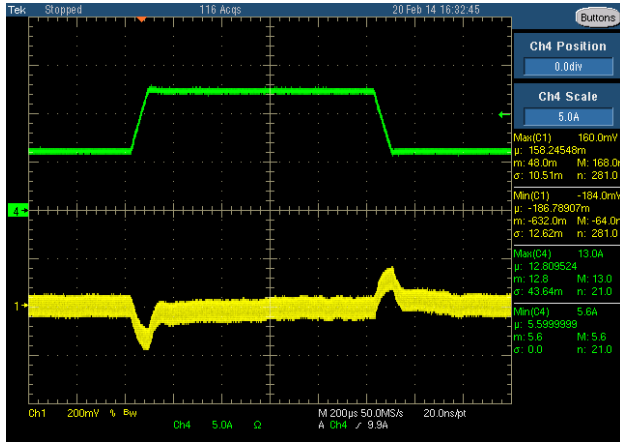


Figure 17. Dynamic Load Transient Waveform (CH1: Output Voltage; CH4: Output Current) at 75 V_{IN} at 25°C Load Step: 25% to 75%

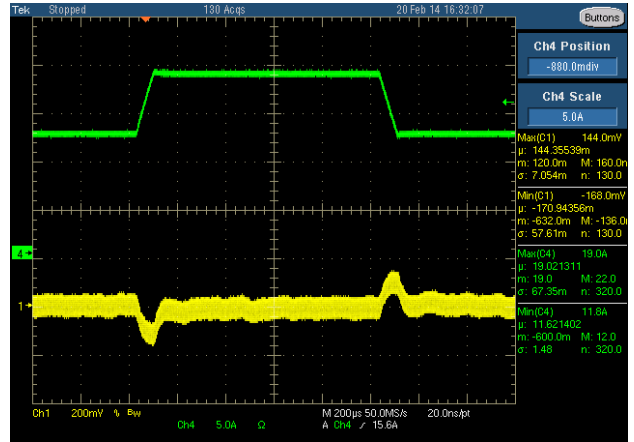


Figure 18. Dynamic Load Transient Waveform (CH1: Output Voltage; CH4: Output Current) at 75 V_{IN} at 25°C Load Step: 25% to 75%

2.5 Turn On Transience

Test condition:

- The unit was tested when turned on by on/off or input from no load to full load.

Pass/fail criteria:

- Rise time < 40 ms

Table 15. Turn on Transience¹

Item	V _{IN} (V)	Load (A)	Specification (ms)			Test Results (ms)		
			Min	Typ	Max	-40°C	+25°C	+85°C
Start Up by On/Off	36	0			100		30.11	
		25					30.15	
	48	0			100		30.00	
		25					30.09	
	75	0			100		29.69	
		25					29.77	
Start Up by Input	36	0			100		29.95	
		25					29.91	
	48	0			100		30.08	
		25					30.00	
	75	0			100		30.08	
		25					30.08	
Pass or Fail						Pass		
Monotonic Waveform when Turned On (Yes/No)						Yes		

¹ CC mode, 0 V sinking threshold as default.

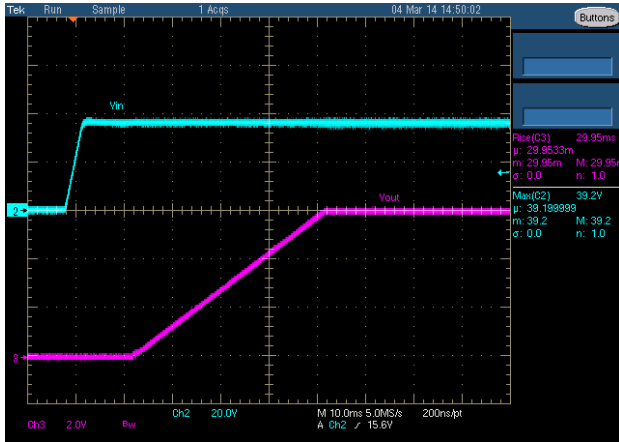


Figure 19. Turn On Transience (CH2: Output Voltage; CH3: Input Voltage/On Off) 36 V_{IN} 0 A V_{IN} Turn On at 25°C

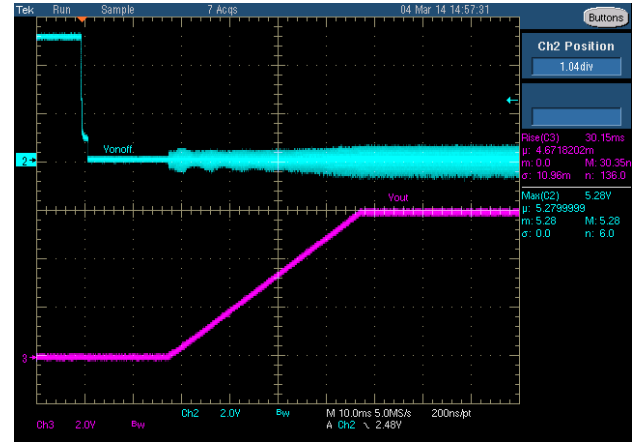


Figure 22. Turn On Transience (CH2: Output Voltage; CH3: Input Voltage/On Off) 36 V_{IN} 25 A On/Off Turn On at 25°C

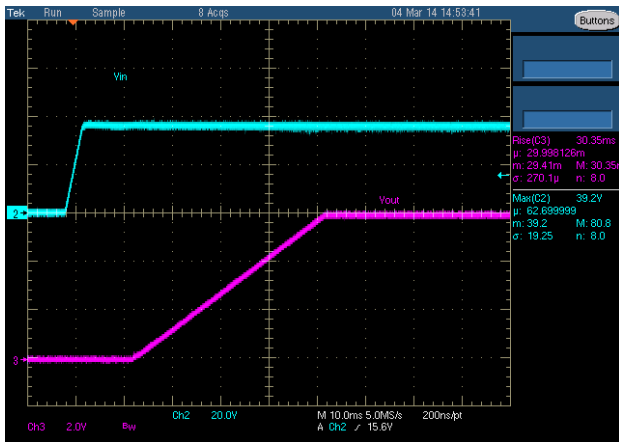


Figure 20. Turn On Transience (CH2: Output Voltage; CH3: Input Voltage/On Off) 36 V_{IN} 25 A V_{IN} Turn on at 25°C

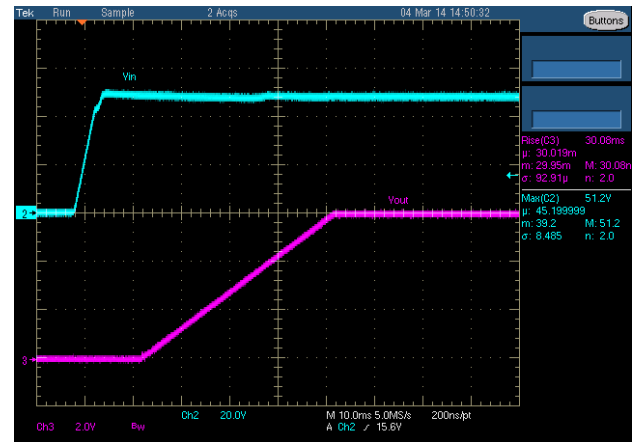


Figure 23. Turn On Transience (CH2: Output Voltage; CH3: Input Voltage/On Off) 48 V_{IN} 0 A V_{IN} Turn On at 25°C

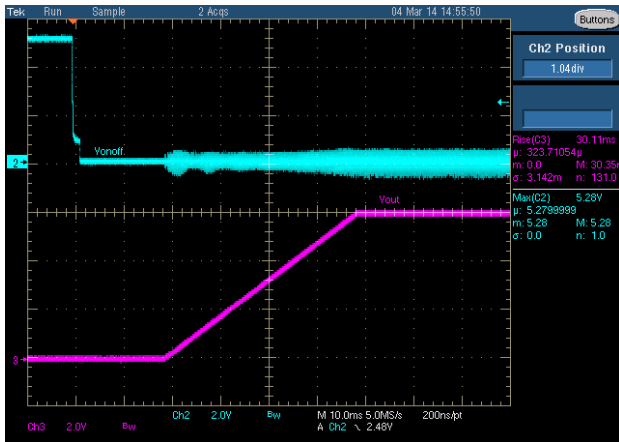


Figure 21. Turn On Transience (CH2: Output Voltage; CH3: Input Voltage/On Off) 36 V_{IN} 0 A On/Off Turn On at 25°C

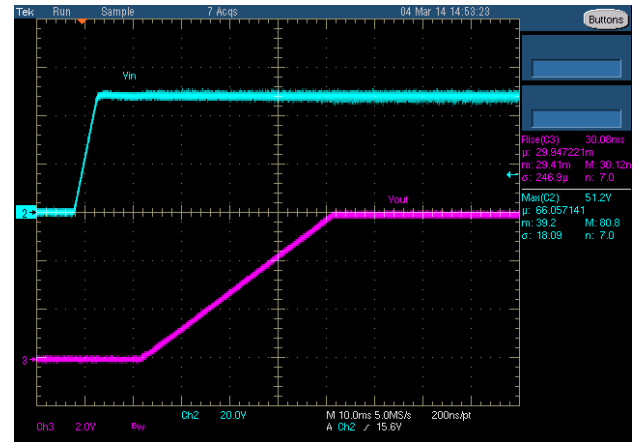


Figure 24. Turn On Transience (CH2: Output Voltage; CH3: Input Voltage/On Off) 48 V_{IN} 25 A V_{IN} Turn On at 25°C

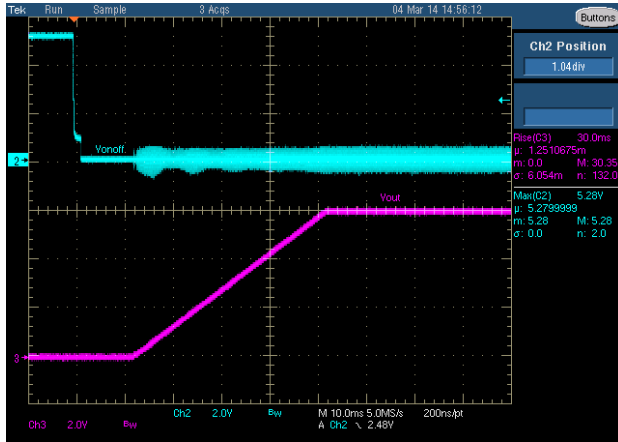


Figure 25. Turn On Transience (CH2: Output Voltage; CH3: Input Voltage/On Off) 48 V_{IN} 0 A On/Off Turn On at 25°C

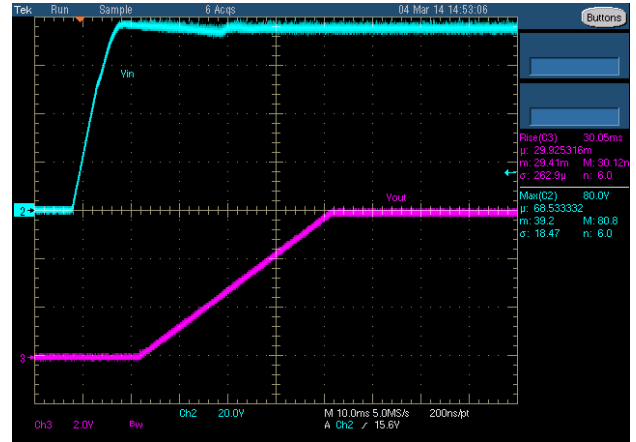


Figure 28. Turn On Transience (CH2: Output Voltage; CH3: Input Voltage/On Off) 75 V_{IN} 25 A V_{IN} Turn On at 25°C

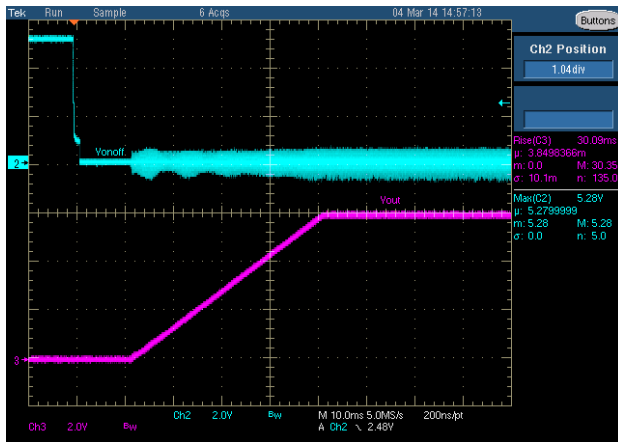


Figure 26. Turn On Transience (CH2: Output Voltage; CH3: Input Voltage/On Off) 48 V_{IN} 25 A On/Off Turn On at 25°C

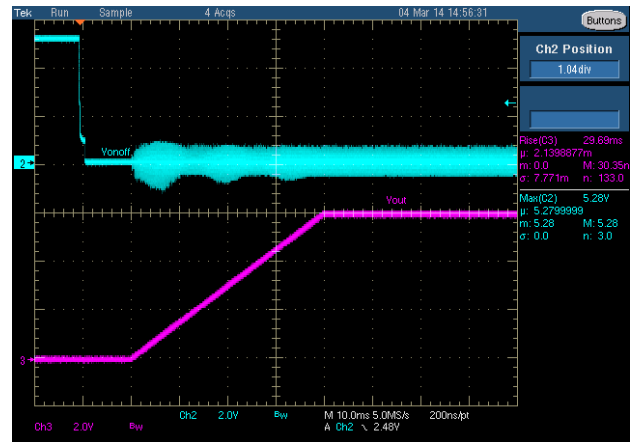


Figure 29. Turn On Transience (CH2: Output Voltage; CH3: Input Voltage/On Off) 75 V_{IN} 0 A On/Off Turn On at 25°C

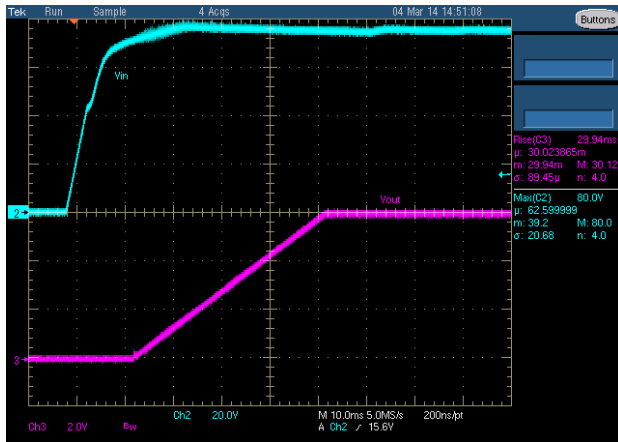


Figure 27. Turn On Transience (CH2: Output Voltage; CH3: Input Voltage/On Off) 75 V_{IN} 0 A V_{IN} Turn On at 25°C

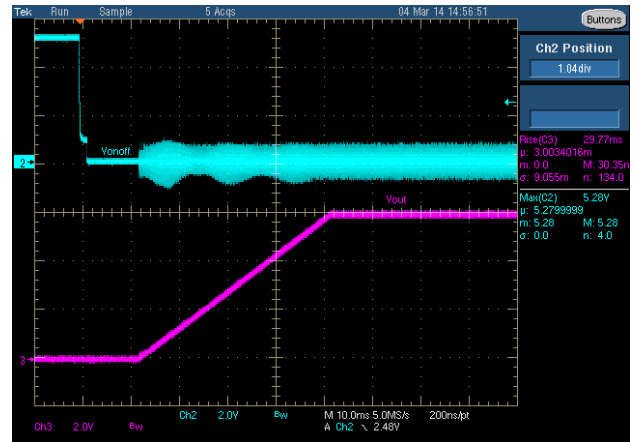


Figure 30. Turn On Transience (CH2: Output Voltage; CH3: Input Voltage/On Off) 75 V_{IN} 25 A On/off Turn On at 25°C

2.6 Turn Off Transience

Test condition:

- The unit was tested when turned off by the on/off pin or input from full load to no load.

Pass/fail criteria:

- Output voltage monotonic drop and no negative current.

Table 16. Turn Off Transience

V _{IN} (V)	Load (A)	Specification	Pass or Fail		
			-40°C	+25°C	+85°C
36	0	Monotonic drop and no negative current		Pass	
48				Pass	
75				Pass	
36	25			Pass	
48				Pass	
75				Pass	
Pass or Fail		Pass			

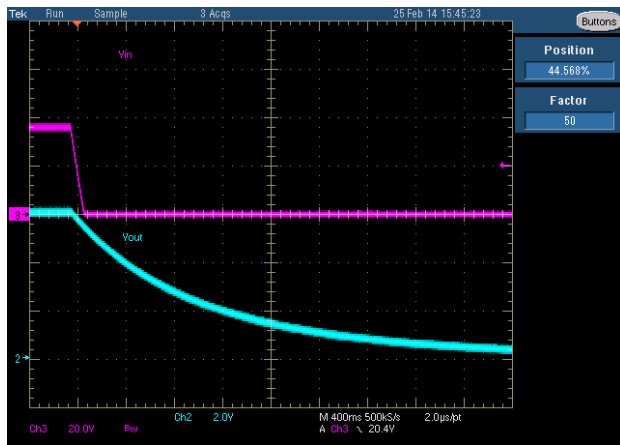


Figure 31. Turn Off Transience (CH2: Output Voltage; CH3: Input Voltage/On Off) at 36 V_{IN} 0 A V_{IN} Turn Off at 25°C

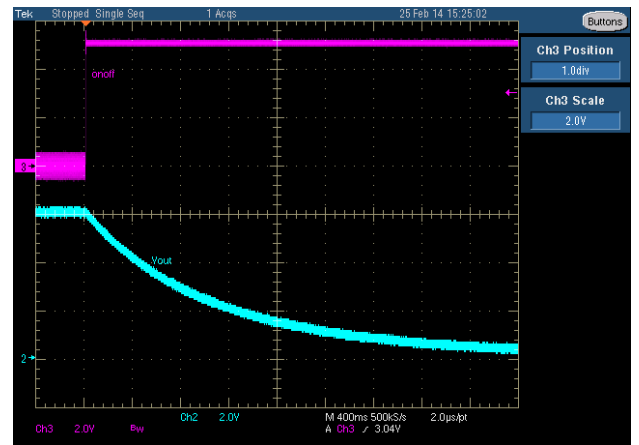


Figure 33. Turn Off Transience (CH2: Output Voltage; CH3: Input Voltage/On Off) at 36 V_{IN} 0 A On/Off Turn Off at 25°C

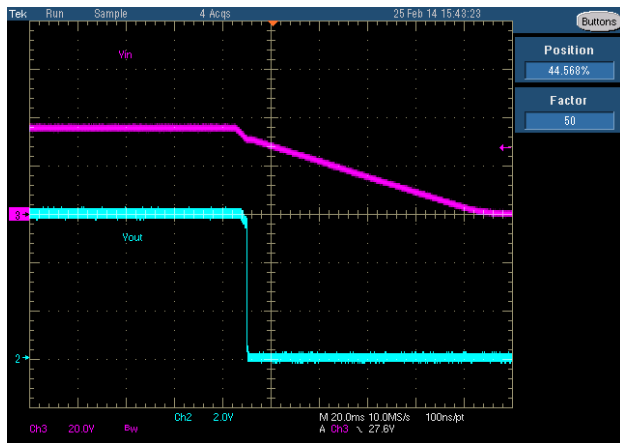


Figure 32. Turn Off Transience (CH2: Output Voltage; CH3: Input Voltage/On Off) at 36 V_{IN} 25 A V_{IN} Turn Off at 25°C

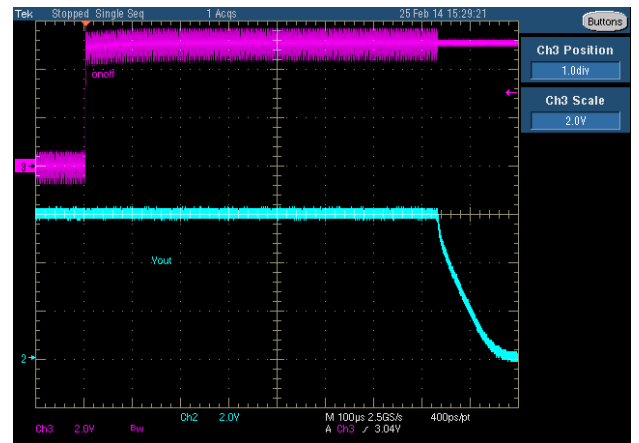


Figure 34. Turn Off Transience (CH2: Output Voltage; CH3: Input Voltage/On Off) at 36 V_{IN} 25 A On/Off Turn Off at 25°C

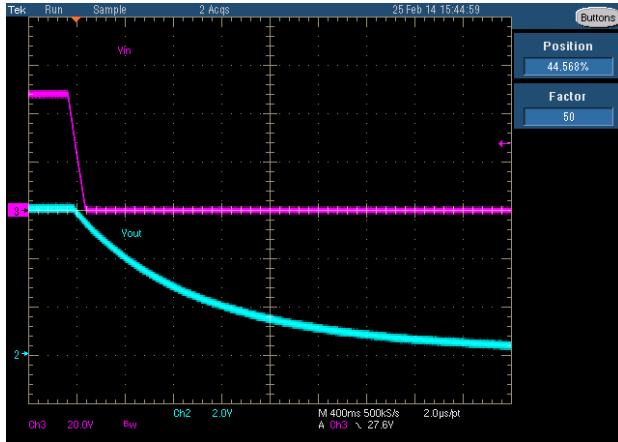


Figure 35. Turn Off Transience (CH2: Output Voltage; CH3: Input Voltage/On Off) at 48 V_{IN} 0 A V_{IN} Turn Off at 25°C

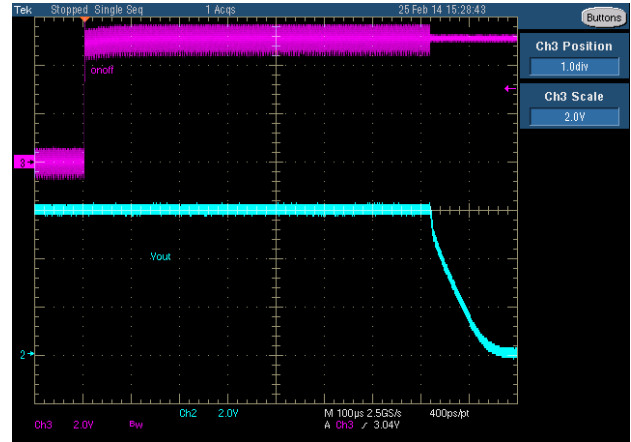


Figure 38. Turn Off Transience (CH2: Output Voltage; CH3: Input Voltage/On Off) at 48 V_{IN} 25 A On/Off Turn Off at 25°C

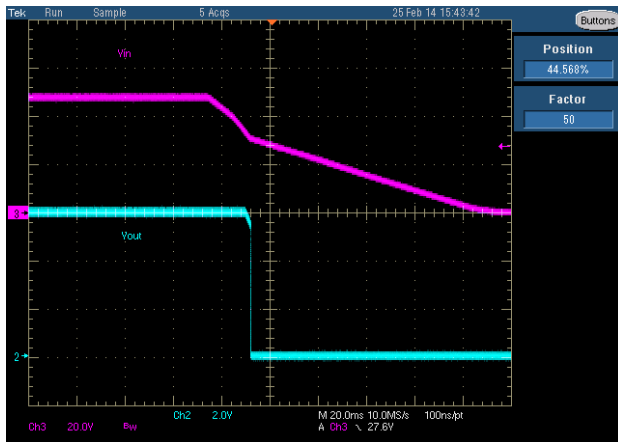


Figure 36. Turn Off Transience (CH2: Output Voltage; CH3: Input Voltage/On Off) at 48 V_{IN} 25 A V_{IN} Turn Off at 25°C

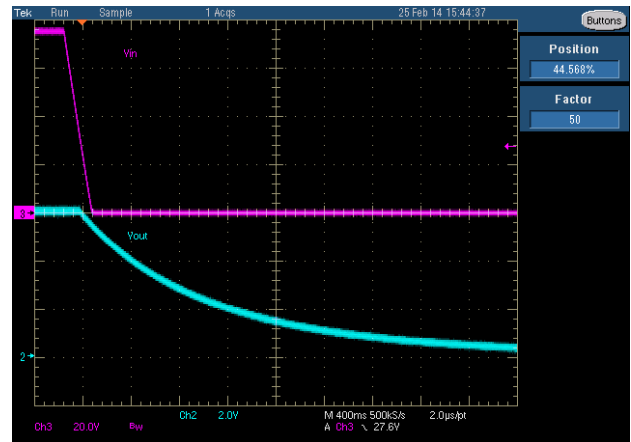


Figure 39. Turn Off Transience (CH2: Output Voltage; CH3: Input Voltage/On Off) at 75 V_{IN} 0 A V_{IN} Turn Off at 25°C

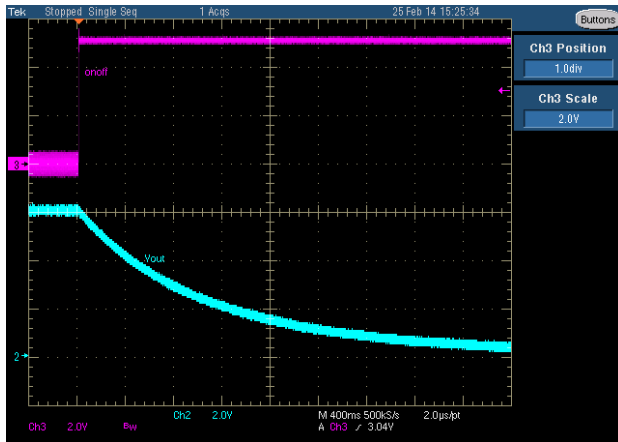


Figure 37. Turn Off Transience (CH2: Output Voltage; CH3: Input Voltage/On Off) at 48 V_{IN} 0 A On/Off Turn Off at 25°C

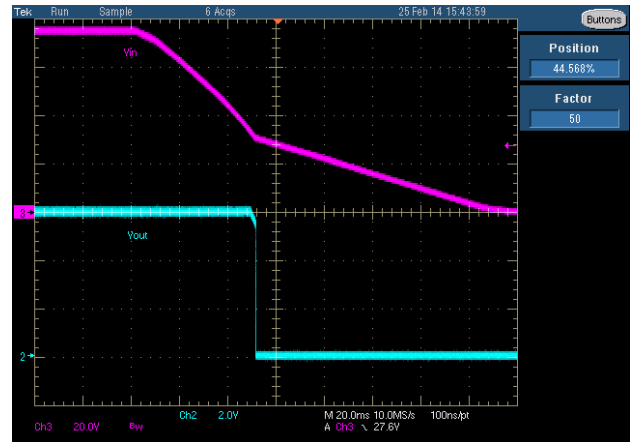


Figure 40. Turn Off Transience (CH2: Output Voltage; CH3: Input Voltage/On Off) at 75 V_{IN} 25 A V_{IN} Turn Off at 25°C

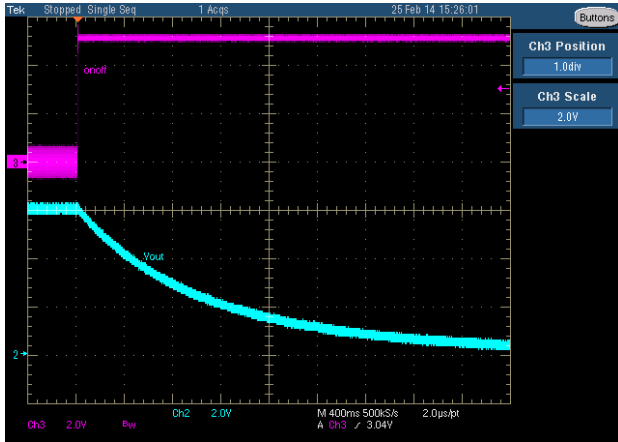


Figure 41. Turn Off Transience (CH2: Output Voltage; CH3: Input Voltage/On Off) at 75 V_{IN} 0 A On/Off Turn Off at 25°C

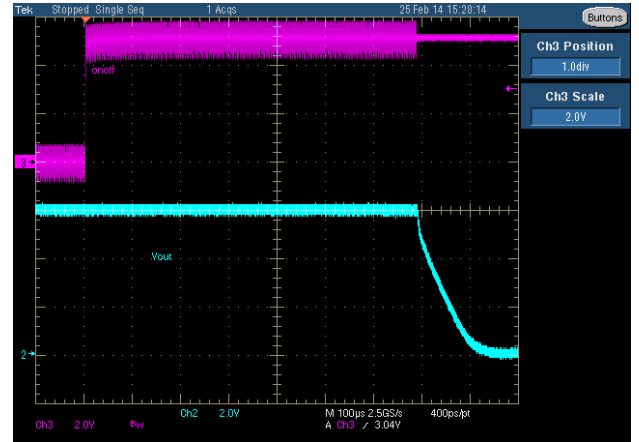


Figure 42. Turn Off Transience (CH2: Output Voltage; CH3: Input Voltage/On Off) at 75 V_{IN} 25 A On/Off Turn Off at 25°C

2.7 Stability

Test condition:

- The loop gain test set at maximum/minimum load at the rated input voltage. Measure feedback loop stability.

Pass/Fail criteria:

- Phase margin shall be greater than 45°. Gain margin shall be less than -12 dB.

Table 17. Loop Stability Margin

V_{IN} (V)	Load (A)	Phase Margin (°)	Test Results (°)			Gain Margin (°)	Test Results (dB)		
			-40°C	+25°C	+85°C		-40°C	+25°C	+85°C
36	0	60		101.6		12		17.7	
48			103.4		17.1				
75			101.9		18.5				
36	25			103.3				17.2	
48				105.0				16.4	
75				105.2				18.1	
Pass or Fail				Pass			Pass		

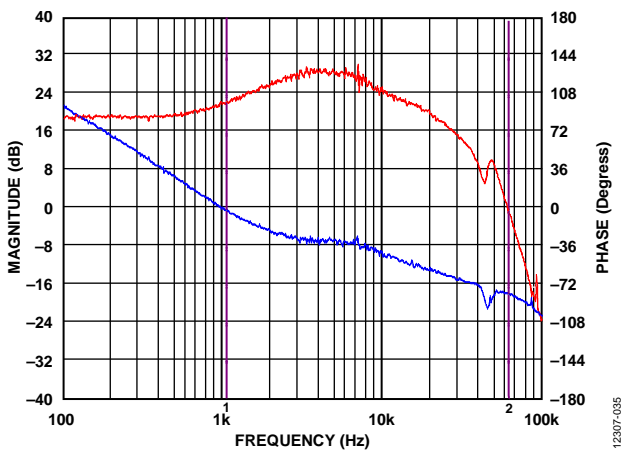


Figure 43. Loop Stability Waveform at 36 V_{IN} , 0 A at 25°C

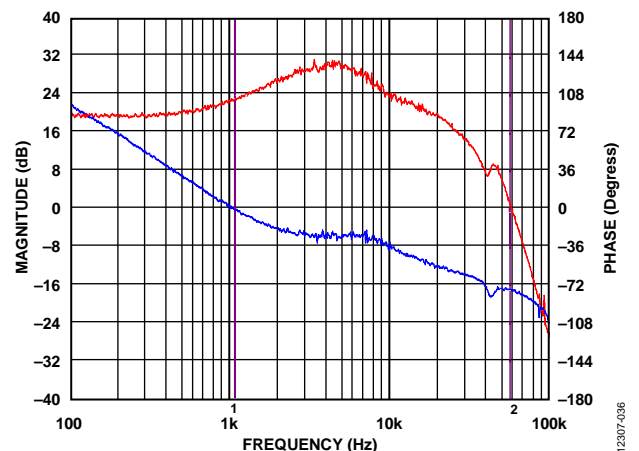


Figure 44. Loop Stability Waveform at 36 V_{IN} , 25 A at 25°C

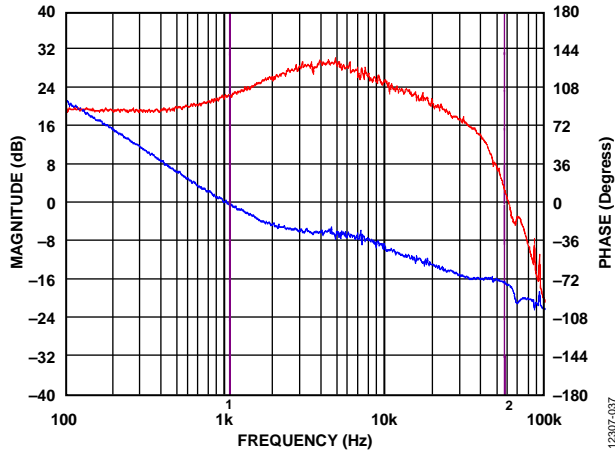


Figure 45. Loop Stability Waveform at 48 V_{IN} , 0 A at 25°C

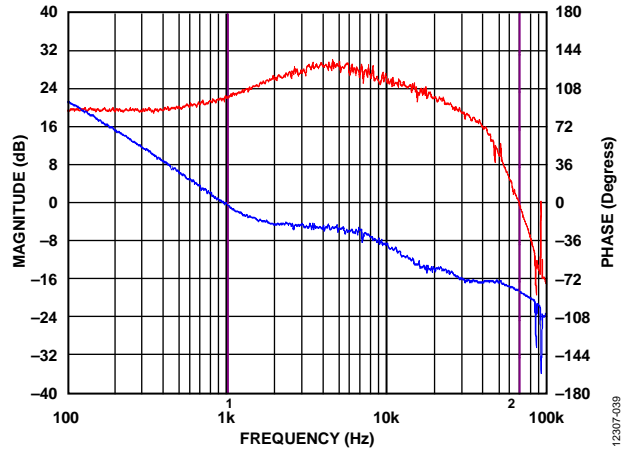


Figure 47. Loop Stability Waveform at 75 V_{IN} , 0 A at 25°C

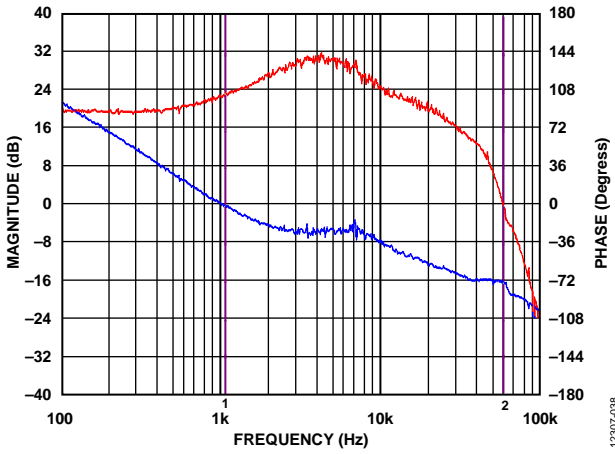


Figure 46. Loop Stability Waveform at 48 V_{IN} , 25 A at 25°C

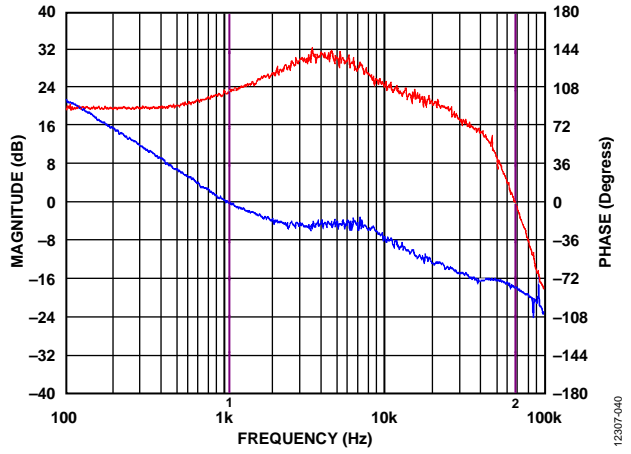


Figure 48. Loop Stability Waveform at 75 V_{IN} , 25 A at 25°C

2.8 Prebias Test

Test condition:

- The unit was tested when turned-on by control.

Pass/fail criteria:

- Output voltage monotonic and smooth startup; reverse current less than 500 mA.

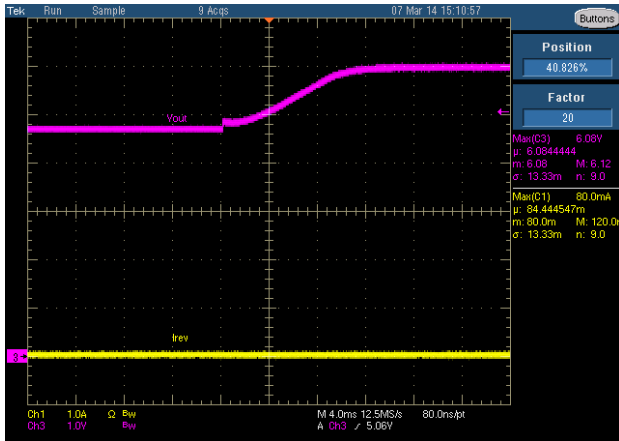


Figure 49. Prebias Waveform (CH1: Reverse Current; CH3: Output Voltage) at 36 V Prebias Soft Start from 4.8 V (0xFE6C[1] = 1, 0xFE39 = 58h)

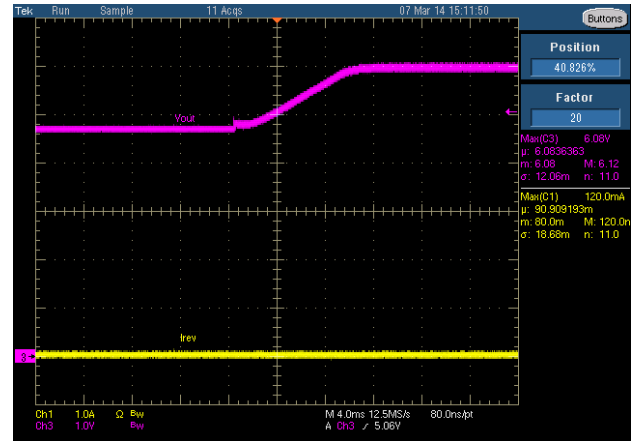


Figure 51. Prebias Waveform (CH1: Reverse Current; CH3: Output Voltage) at 60 V Prebias Soft Start from 4.8 V (0xFE6C[1] = 1, 0xFE39 = 58h)

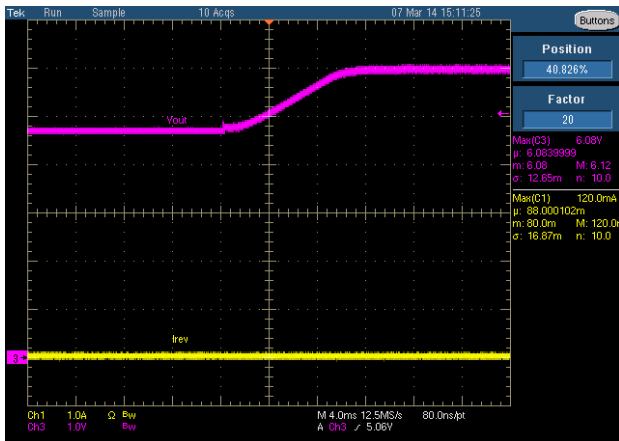


Figure 50. Prebias Waveform (CH1: Reverse Current; CH3: Output Voltage) at 48 V Prebias Soft Start from 4.8 V (0xFE6C[1] = 1, 0xFE39 = 58h)

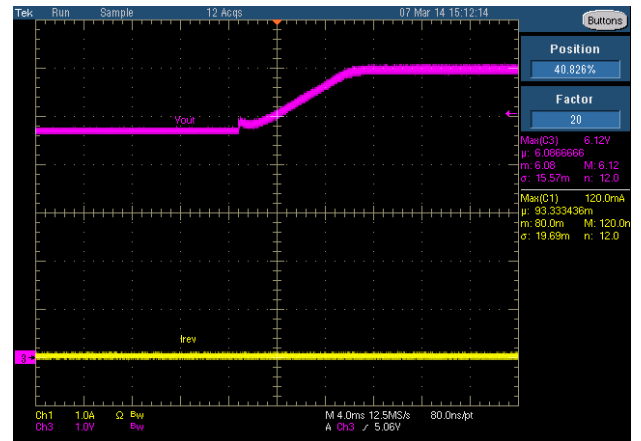


Figure 52. Prebias Waveform (CH1: Reverse Current; CH3: Output Voltage) at 75 V Prebias Soft Start from 4.8 V (0xFE6C[1] = 1, 0xFE39 = 58h)

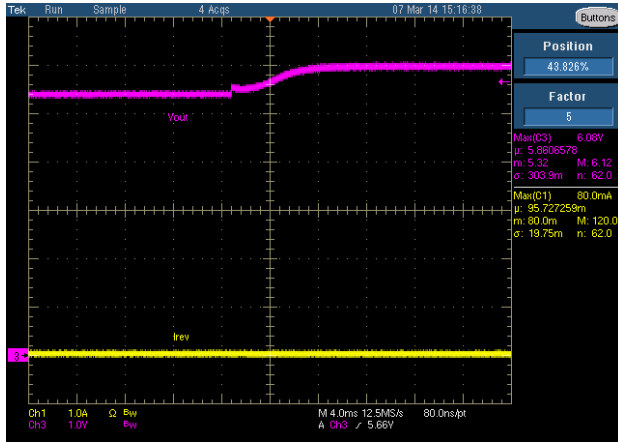


Figure 53. Prebias Waveform (CH1: Reverse Current; CH3: Output Voltage) at 36 V Prebias Soft Start from 5.4 V (0xFE6C[1] = 1, 0xFE39 = 58h)

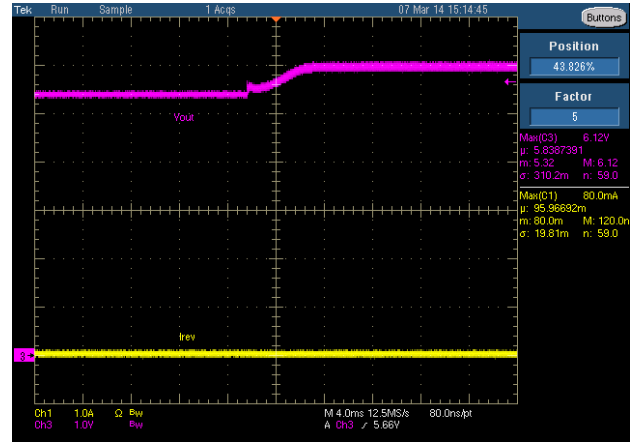


Figure 56. Prebias Waveform (CH1: Reverse Current; CH3: Output Voltage) at 75 V Prebias Soft Start from 5.4 V (0xFE6C[1] = 1, 0xFE39 = 58h)

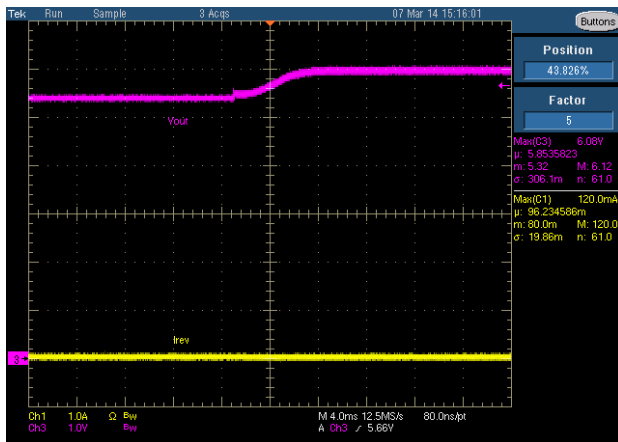


Figure 54. Prebias Waveform (CH1: Reverse Current; CH3: Output Voltage) at 48 V Prebias Soft Start from 5.4 V (0xFE6C[1] = 1, 0xFE39 = 58h)



Figure 57. Prebias Waveform (CH1: Reverse Current; CH3: Output Voltage) at 36 V Prebias Soft Start from 6.0 V (0xFE6C[1] = 1, 0xFE39 = 58h)

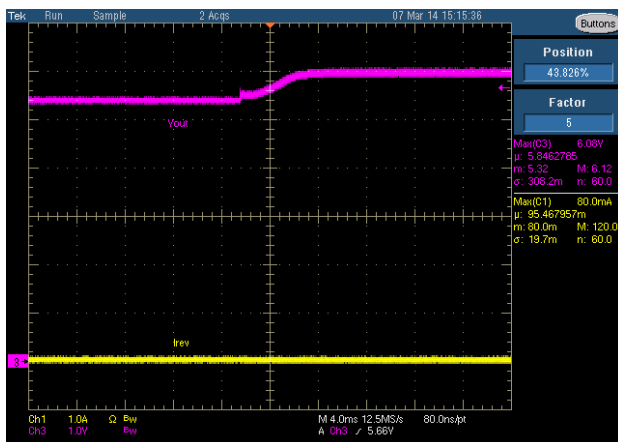


Figure 55. Prebias Waveform (CH1: Reverse Current; CH3: Output Voltage) at 60 V Prebias Soft Start from 5.4 V (0xFE6C[1] = 1, 0xFE39 = 58h)

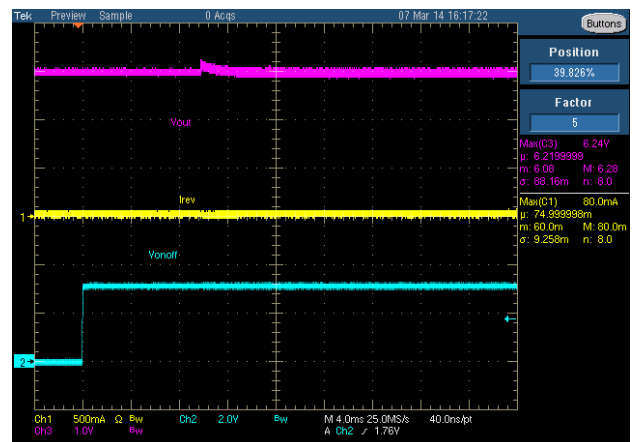


Figure 58. Prebias Waveform (CH1: Reverse Current; CH3: Output Voltage) at 48 V Prebias Soft Start from 6.0 V (0xFE6C[1] = 1, 0xFE39 = 58h)

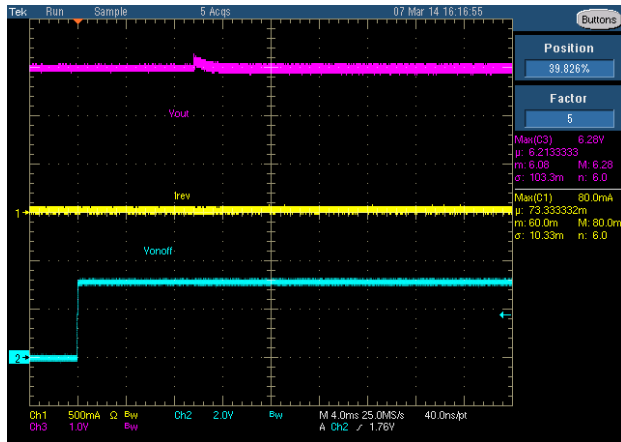


Figure 59. Prebias Waveform (CH1: Reverse Current; CH3: Output Voltage) at 60 V Prebias Soft Start from 6.0 V (0xFE6C[1] = 1, 0xFE39 = 58h)

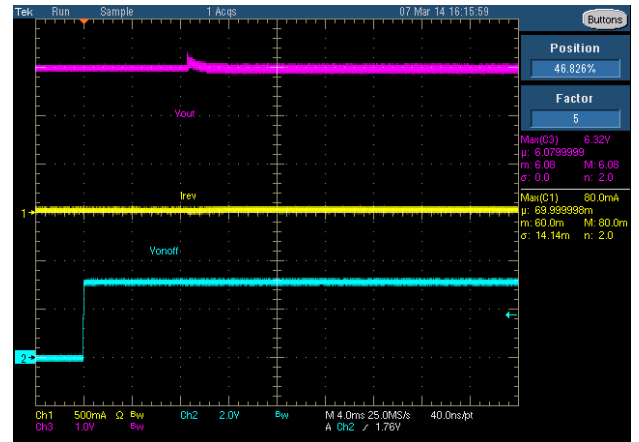


Figure 60. Prebias Waveform (CH1: Reverse Current; CH3: Output Voltage) at 75 V Prebias Soft Start from 6.0 V (0xFE6C[1] = 1, 0xFE39 = 58h)

Protection

3.1 Output Overcurrent Protection (Output OCP)

Test condition:

- The load is increased to an estimated overcurrent value in several steps. The test is repeated with different input voltages.

Pass/fail criteria:

- The unit test shall meet the specification requirements.

Table 18. OCP Threshold

V _{IN} (V)	Specification (A)			Value (A)		
	Min	Typ	Max	-40°C	+25°C	+85°C
36		32			35.3	
48		32			32.9	
75		32			28.6	
Pass or Fail		Pass				

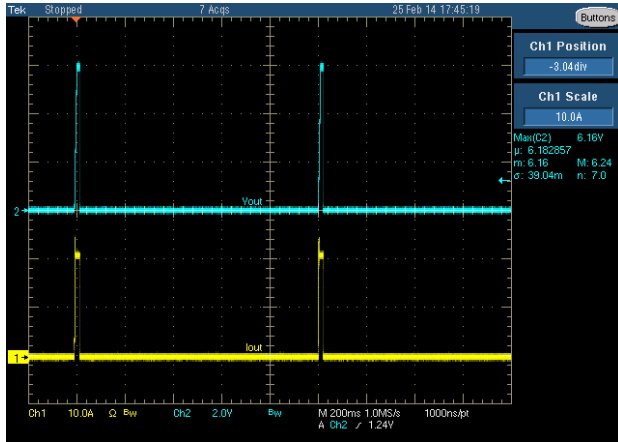


Figure 61. OCP Hiccup (CH2: Output Voltage; CH1: Output Current) at 36 V_{IN} at 25°C

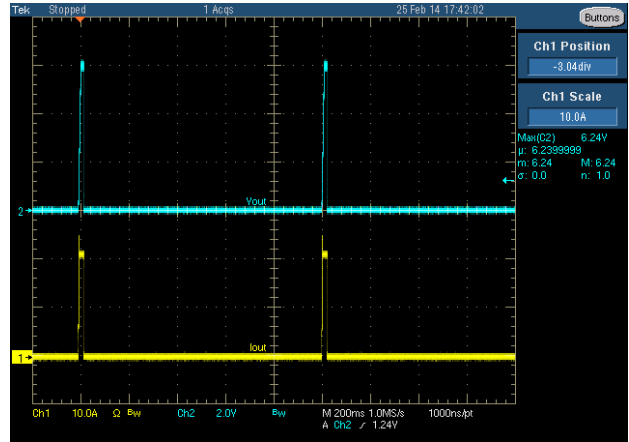


Figure 63. OCP Hiccup (CH2: Output Voltage; CH1: Output Current) at 75 V_{IN} at 25°C

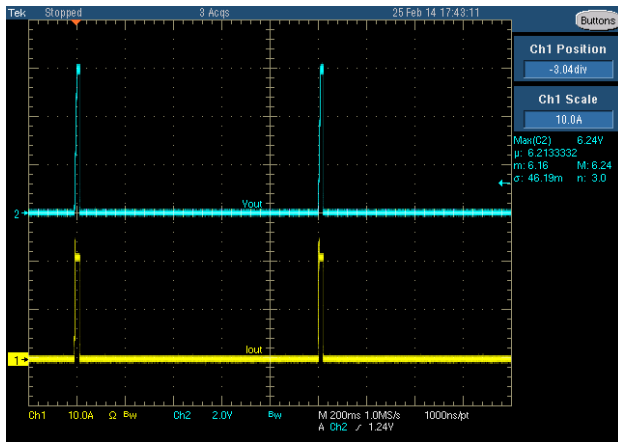


Figure 62. OCP Hiccup (CH2: Output Voltage; CH1: Output Current) at 48 V_{IN} at 25°C

3.2 Output Short-Circuit Protection (Output SCP)

Test condition:

- A short circuit is defined as less than 0.1 Ω resistance between the output terminals.

Pass/fail criteria:

- The unit test shall meet the specification requirements.

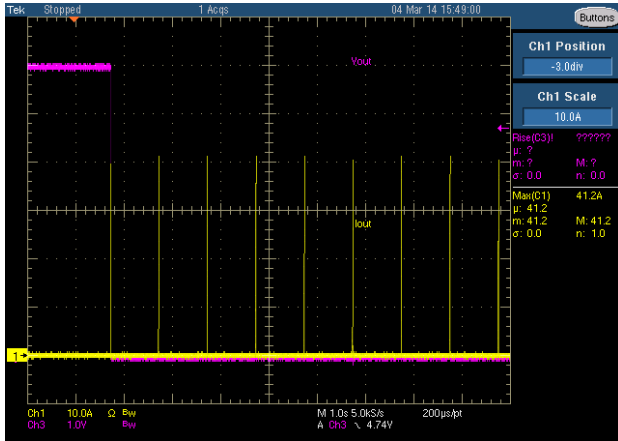


Figure 64. SCP Hiccup (CH2: Output Voltage CH4: Output Current) at 36 V_{IN} Turn On at No Load Then Short at 25°C

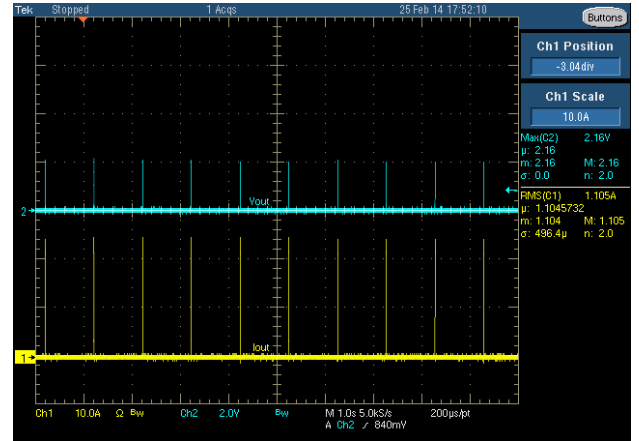


Figure 66. SCP Hiccup (CH2: Output Voltage CH4: Output Current) at 36 V_{IN} Short Then Turn On at 25°C

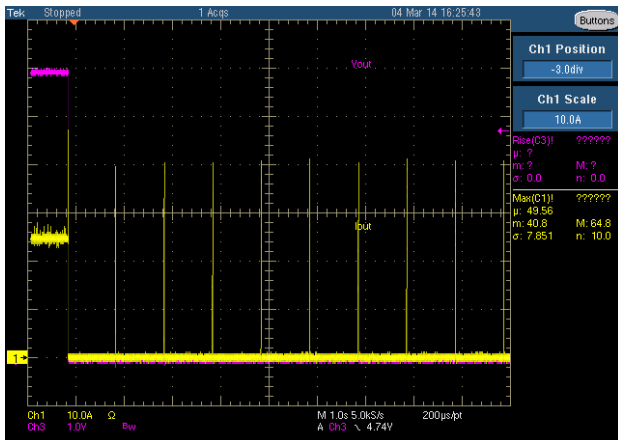


Figure 65. SCP Hiccup (CH2: Output Voltage CH4: Output Current) at 36 V_{IN} Turn On Full Load Then Short at 25°C

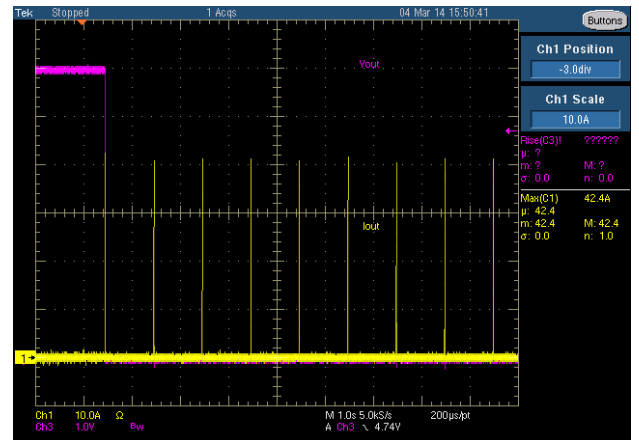


Figure 67. SCP Hiccup (CH2: Output Voltage CH4: Output Current) at 48 V_{IN} Turn On at No Load Then Short at 25°C

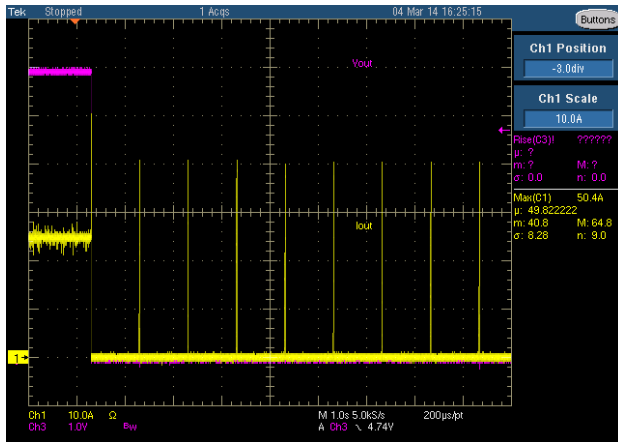


Figure 68. SCP Hiccup (CH2: Output Voltage CH4: Output Current) at 48 V_{IN} Turn On Full Load Then Short at 25°C

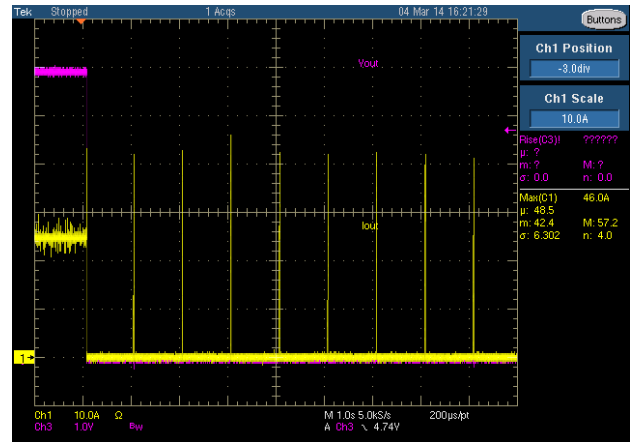


Figure 71. SCP Hiccup (CH2: Output Voltage CH4: Output Current) at 75 V_{IN} Turn On Full Load Then Short at 25°C

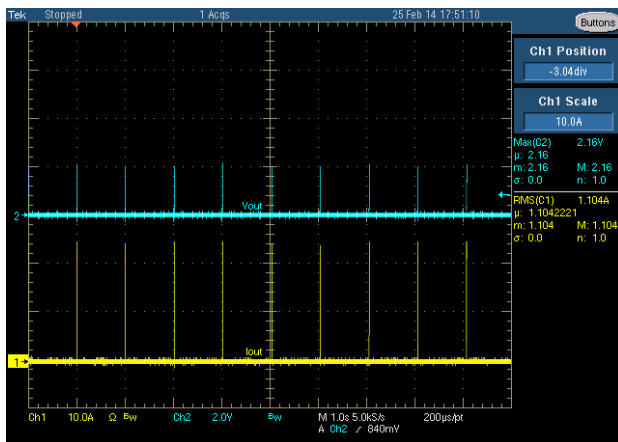


Figure 69. SCP Hiccup (CH2: Output Voltage CH4: Output Current) at 48 V_{IN} Short Then Turn On at 25°C

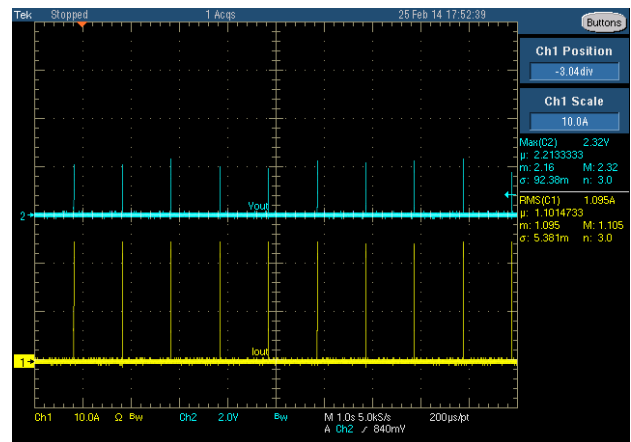


Figure 72. SCP Hiccup (CH2: Output Voltage CH4: Output Current) at 75 V_{IN} Short Then Turn On at 25°C

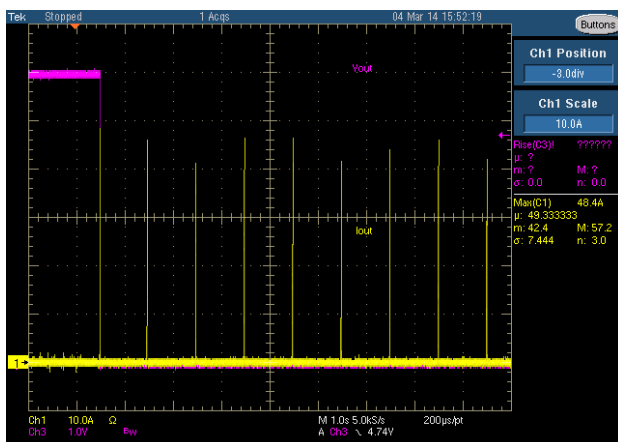


Figure 70. SCP Hiccup (CH2: Output Voltage CH4: Output Current) at 75 V_{IN} Turn On at No Load Then Short at 25°C

3.3 Output Overvoltage Protection (Output OVP)

Test condition:

- Short the lower resistor of feedback divider network.

Pass/fail criteria:

- The unit test shall meet the specification requirements.

Table 19. OVP Threshold

V _{IN} (V)	Load (A)	Specification (V)	Test Results (V)		
			-40°C	+25°C	+85°C
36	0	7.00		6.64	
48			6.64		
75			6.48		
36	25			6.88	
48			6.96		
75			6.88		
Pass or Fail				Pass	

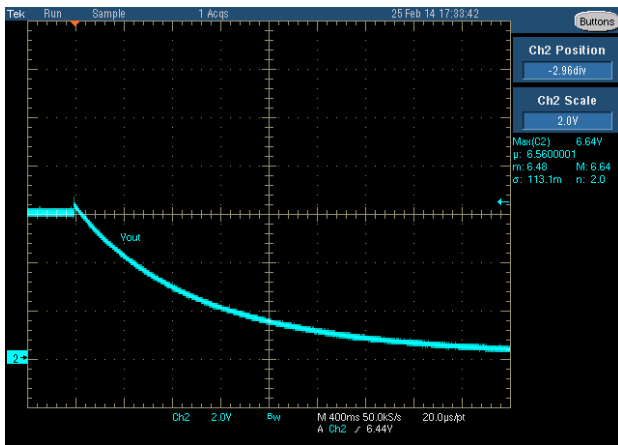


Figure 73. OVP Threshold (CH2: Output Voltage) at 36 V_{IN}, 0 A at 25°C

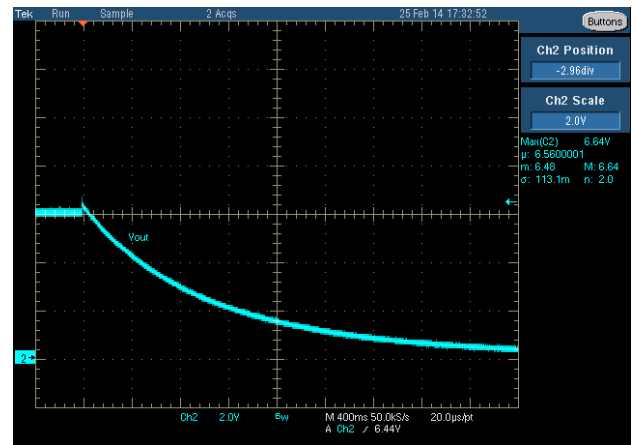


Figure 75. OVP Threshold (CH2: Output Voltage) at 48 V_{IN}, 0 A at 25°C

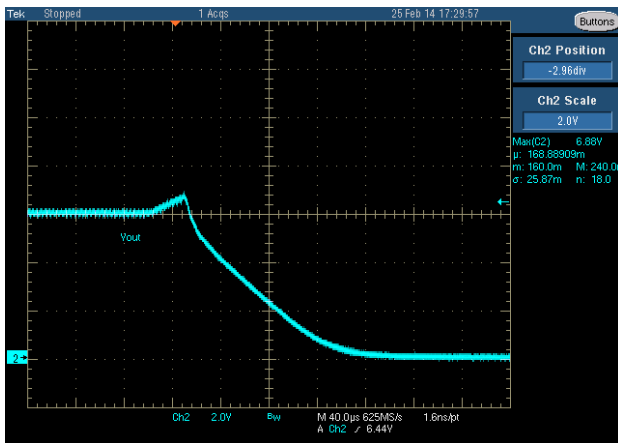


Figure 74. OVP Threshold (CH2: Output Voltage) at 36 V_{IN}, 25 A at 25°C

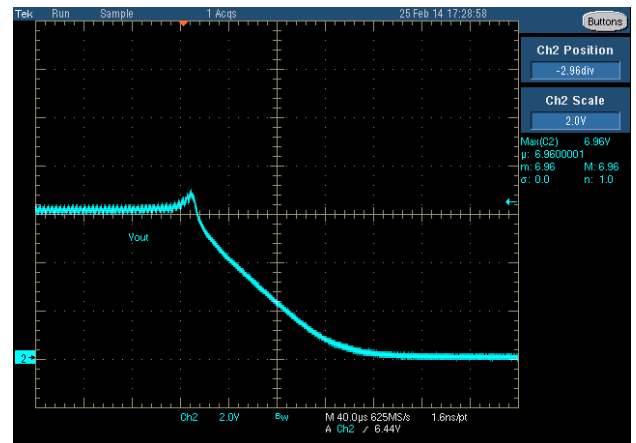


Figure 76. OVP Threshold (CH2: Output Voltage) at 48 V_{IN}, 25 A at 25°C

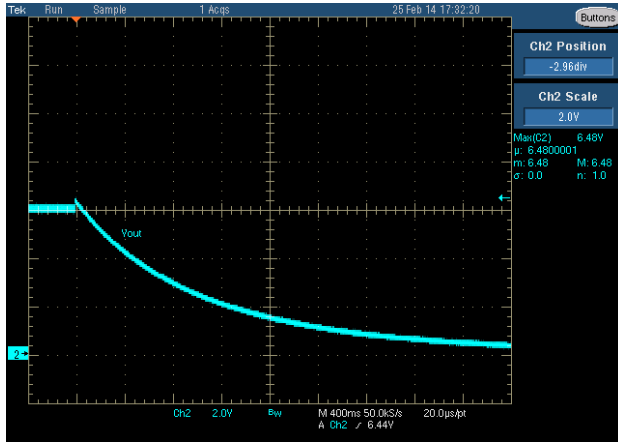


Figure 77. OVP Threshold (CH2: Output Voltage) at 75 V_{IN}, 0 A at 25°C

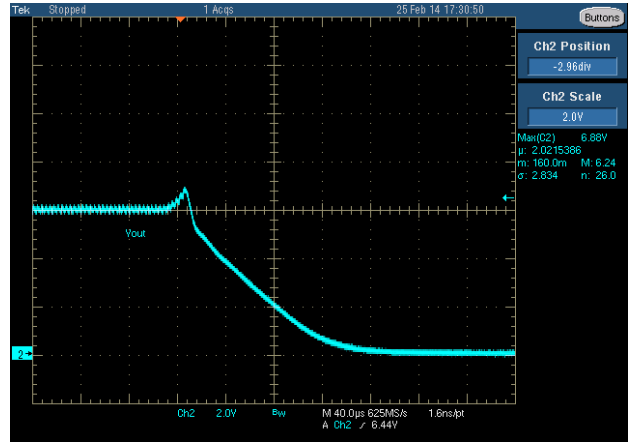


Figure 78. OVP Threshold (CH2: Output Voltage) at 75 V_{IN}, 25 A at 25°C

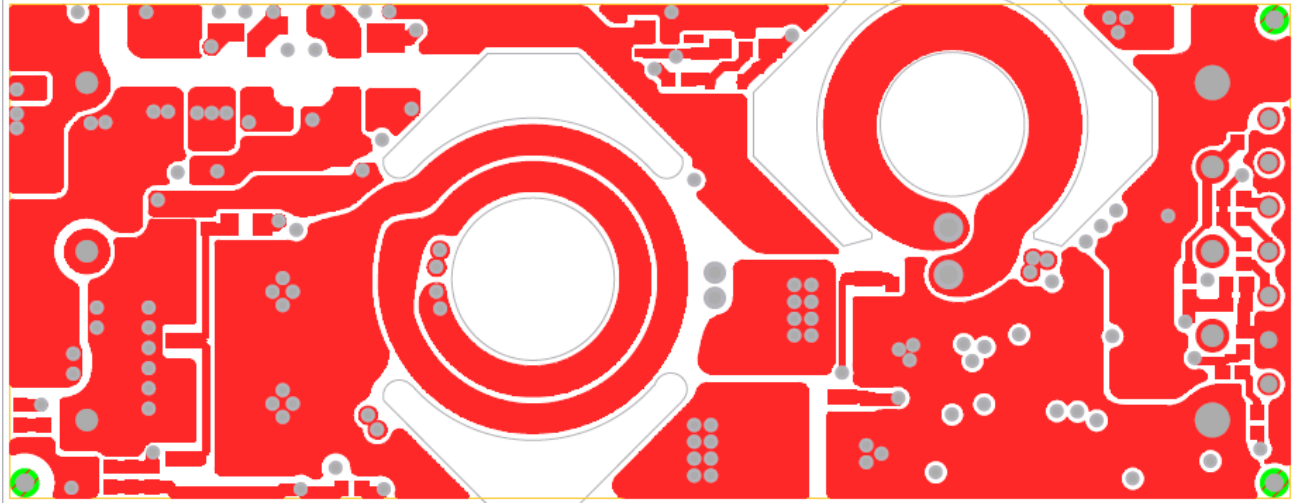


Figure 80. Layer 1

12307-004

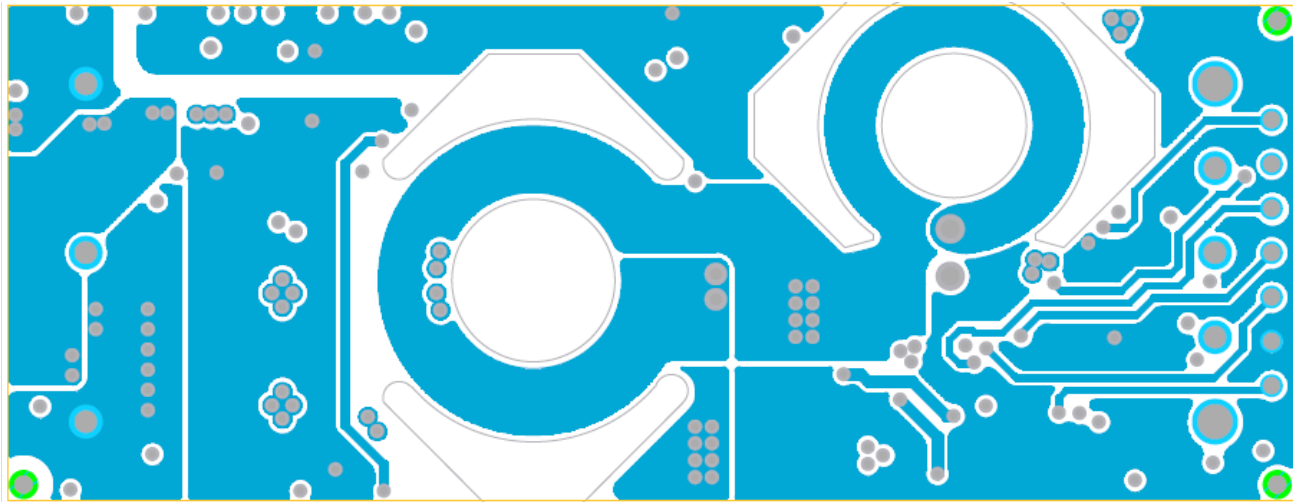


Figure 81. Layer 2

12307-005

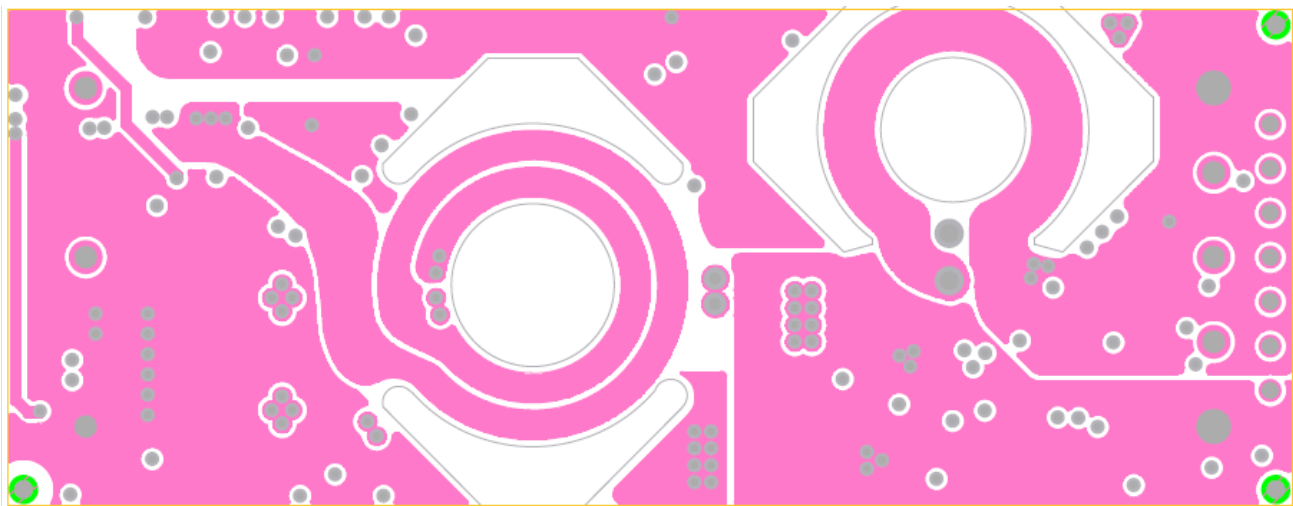
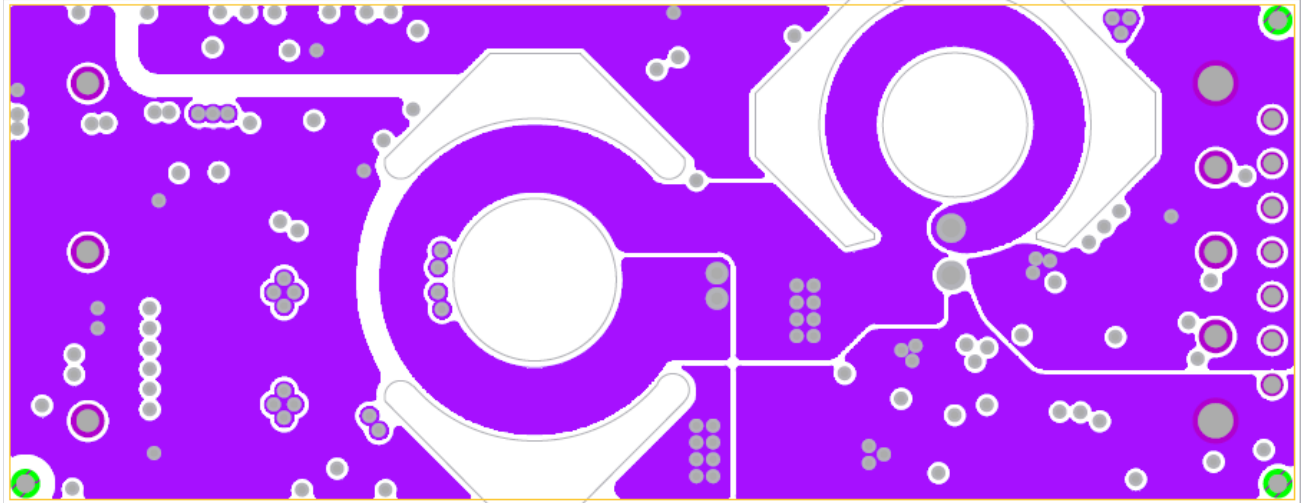


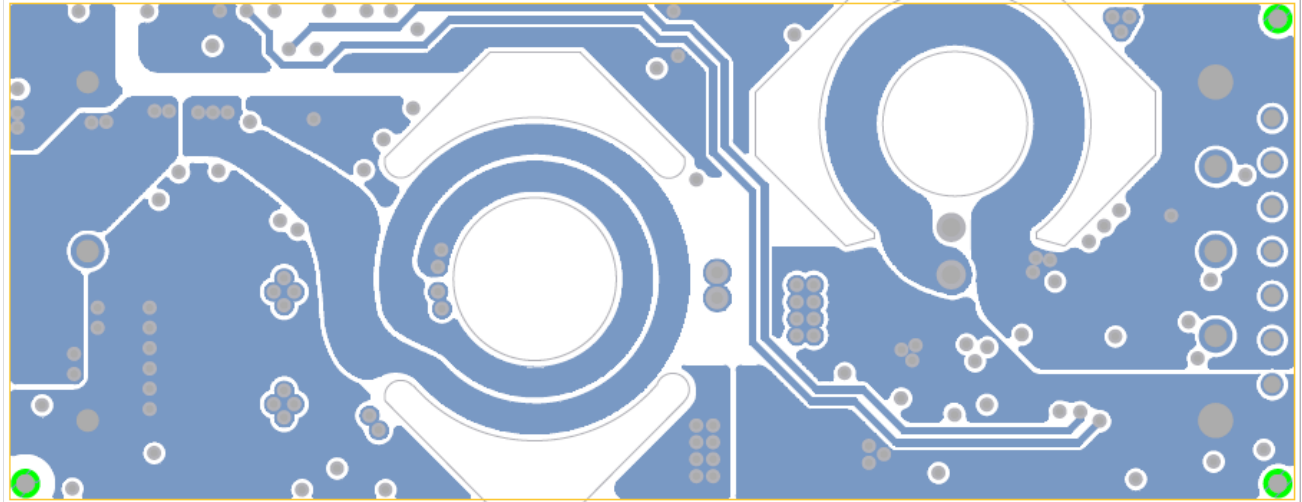
Figure 82. Layer 3

12307-006



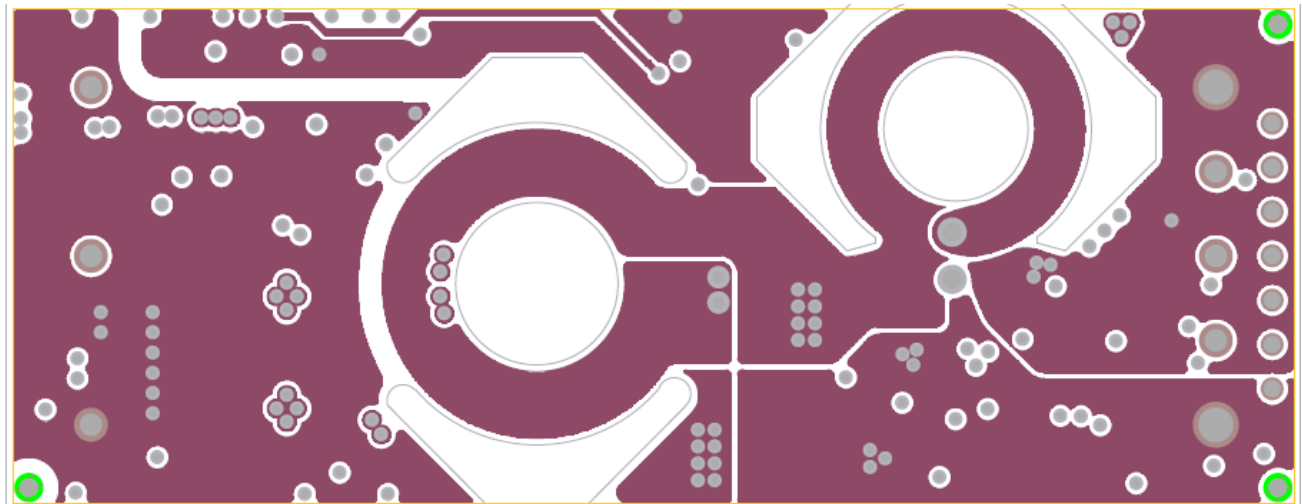
12307-007

Figure 83. Layer 4



12307-008

Figure 84. Layer 5



12307-009

Figure 85. Layer 6

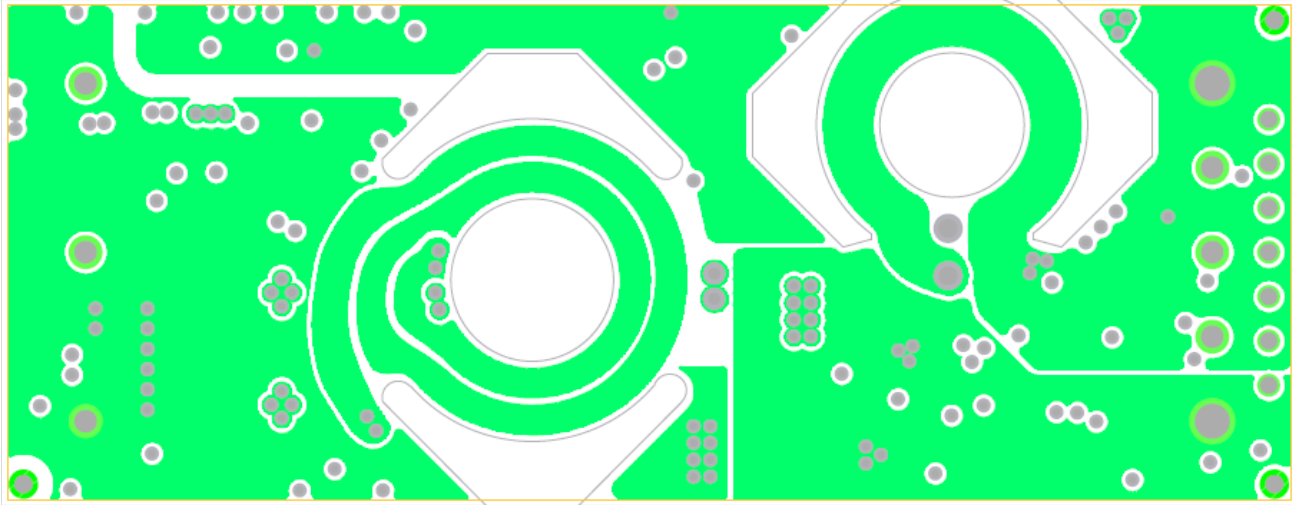


Figure 86. Layer 7

12307-010

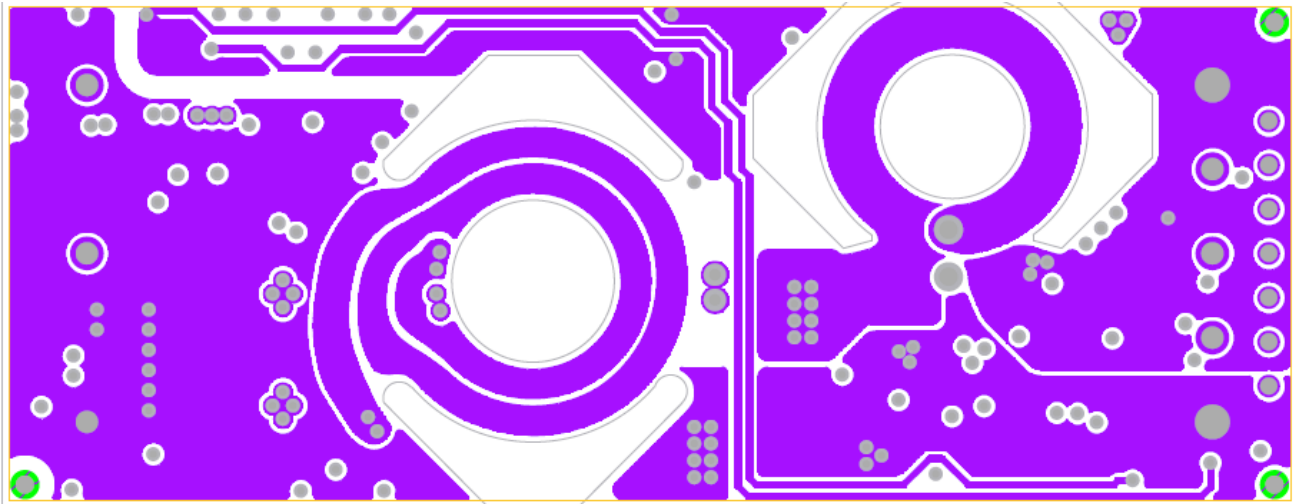


Figure 87. Layer 8

12307-011

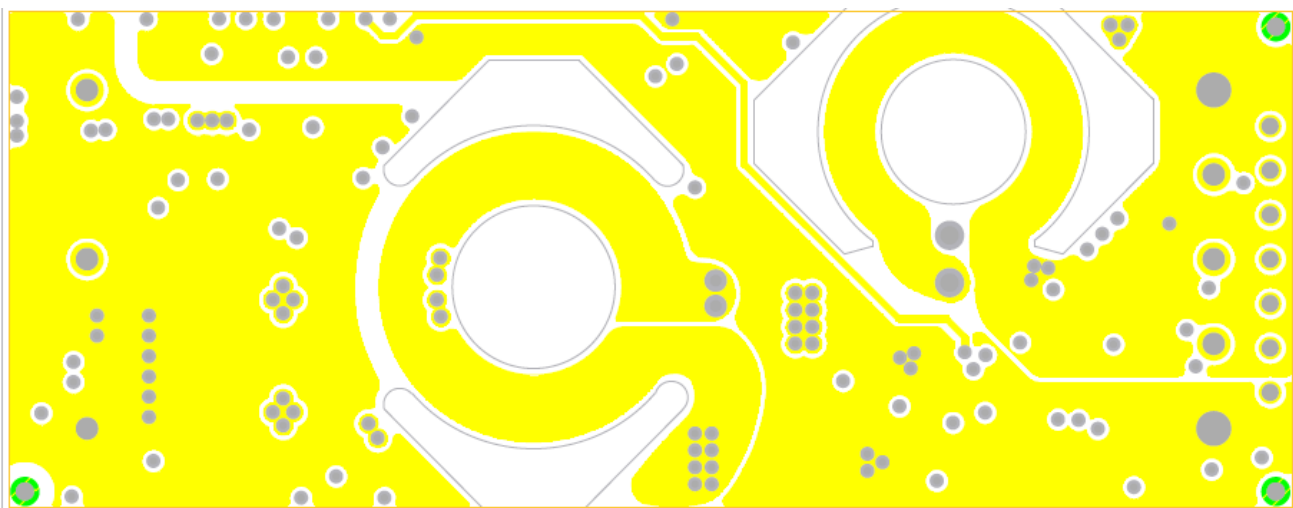
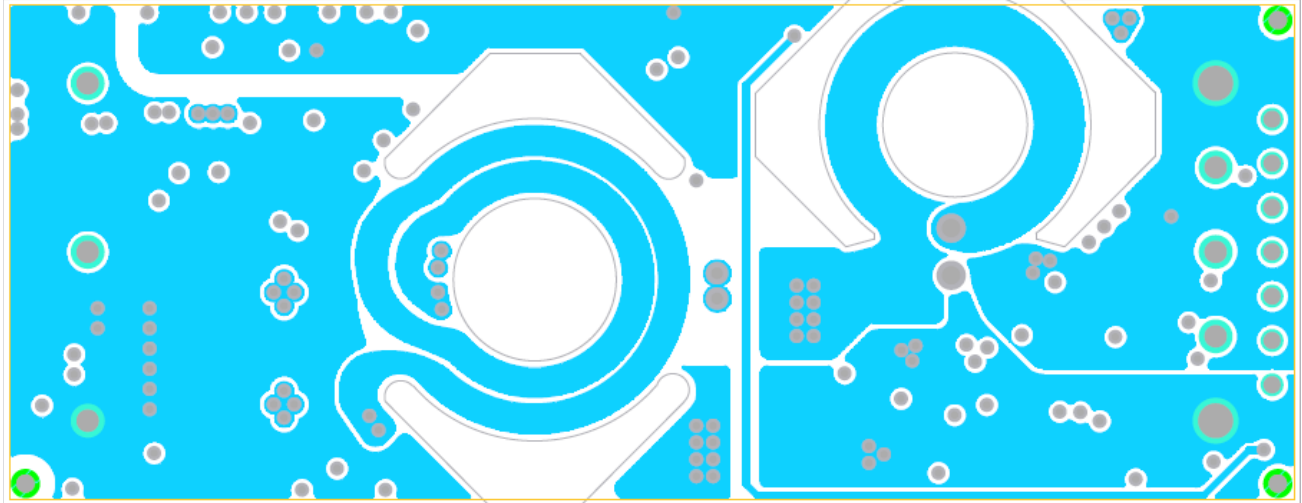


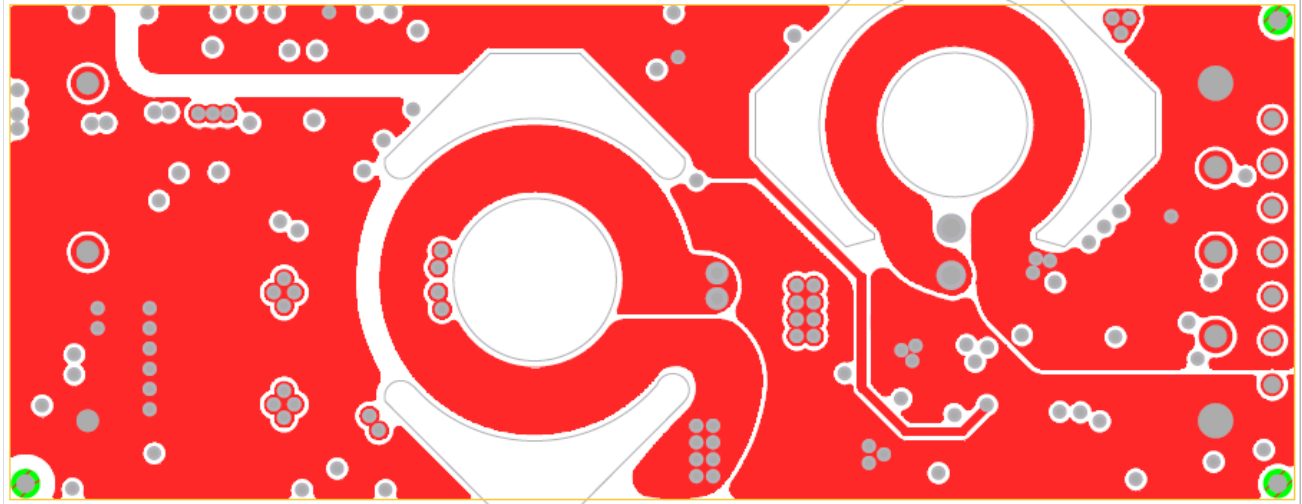
Figure 88. Layer 9

12307-012



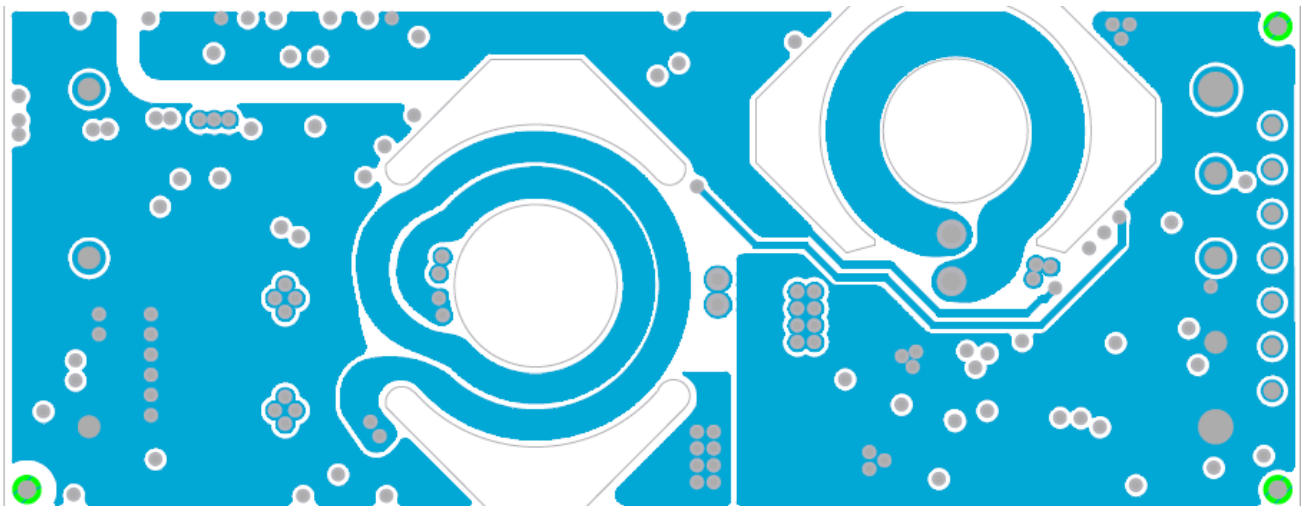
12307-013

Figure 89. Layer 10



12307-014

Figure 90. Layer 11



12307-015

Figure 91. Layer 12

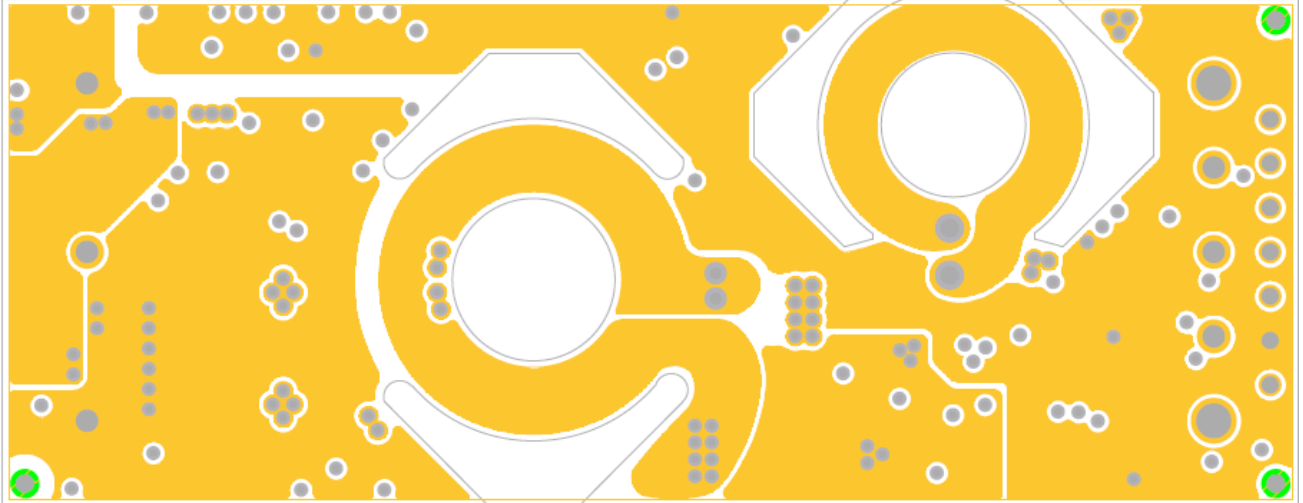


Figure 92. Layer 13

12307-016

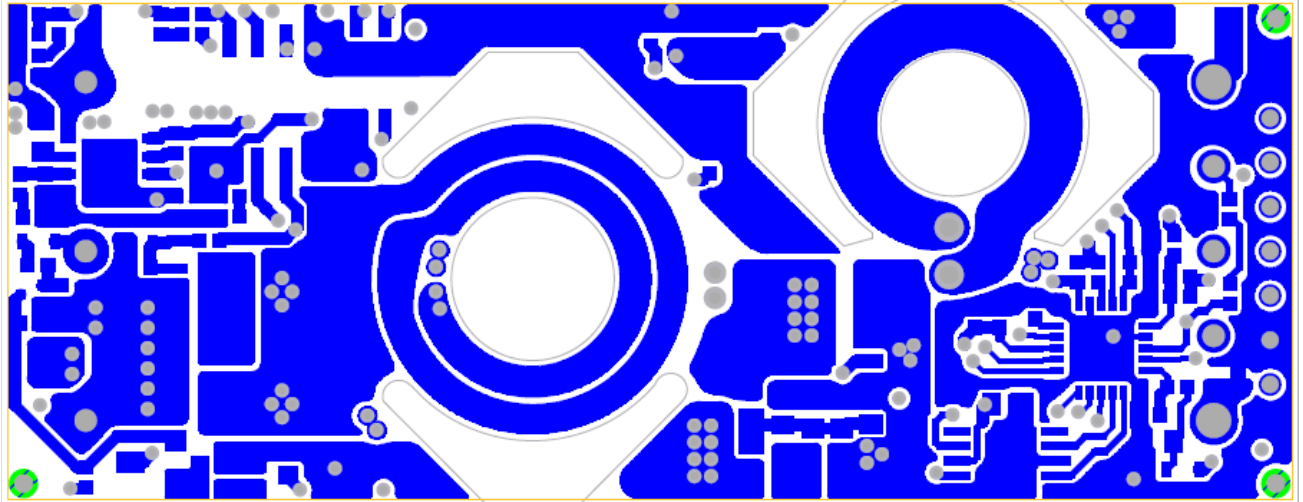


Figure 93. Layer 14

12307-017

ORDERING INFORMATION

BILL OF MATERIALS

Table 20.

Qty	Ref	Part Number	Value	Description	Vendor	Package
1	C90	C1206C102MGRACTU	1 nF/2000 V	Capacitor, ceramic, 1000 pF, 2 kV, 20%, X7R, 1206	Kemet	C1206
3	C101, C102, C106	12061Z475KAT2A	4.7 μ F/100 V	Capacitor, ceramic, 4.7 μ F, 100 V, 10% X7S, 1206	AVX	C1206
1	C103	C3216X7R2E683K160AA	68 nF/250 V	Capacitor, ceramic, 0.068 μ F, 250 V, X7R, 1206	TDK	C1206
3	C104, C306, C509	C1005X7R1C104M050BC	0.1 μ F/16 V	Capacitor, ceramic, 0.1 μ F, 16 V, 20%, X7R, 0402	TDK	C0402
4	C105, C107, C502, C505	C1608X7R1C105M080AC	1 μ F/16 V	Capacitor, ceramic, 1 μ F, 16 V, 20%, X7R, 0603	TDK	C0603
3	C201, C204, C508	C1005X7R1E103K050BB	10 nF/25 V	Capacitor, ceramic, 10000 pF, 25 V, 10%, X7R, 0402	TDK	C0402
1	C202	C1005X7R1E104K050BB	0.1 μ F/25 V	Capacitor, ceramic, 0.1 μ F, 25 V, 10%, X7R, 0402	TDK	C0402
1	C203	C1005C0G1H101K050BA	100 pF/50 V	Capacitor, ceramic, 100 pF, 50 V, 10%, NP0, 0402	TDK	C0402
5	C205, C206, C210, C212, C305	C1005C0G1H102K050BA	1 nF/50 V	Capacitor, ceramic, 1000 pF, 50 V, 10%, NP0, 0402	TDK	C0402
1	C207	C1608X7S2A104K080AB	100 nF/100 V	Capacitor, ceramic, 0.1 μ F, 100 V, 10%, X7S, 0603	TDK	C0603
1	C208	C1005X7S1A225K050BC	2.2 μ F/10 V	Capacitor, ceramic, 2.2 μ F, 10 V, 10%, X7S, 0402	TDK	C0402
1	C209	C1005X7S1A334K050BC	0.33 μ F/10 V	Capacitor, ceramic, 0.33 μ F, 10 V, 10%, X7S, 0402	TDK	C0402
1	C211	C0402C101J1GACTU	100 pF/100 V	Capacitor, ceramic, 100 pF, 100 V, 5%, NP0, 0402	KEMET	C0402
1	C301	C1005X7R1H221M050BA	220 pF/50 V	Capacitor, ceramic, 220 pF, 50 V, 20%, X7R, 0402	TDK	C0402
1	C302	C1608X7R1E105K080AB	1 μ F/25 V	Capacitor, ceramic, 1 μ F, 25 V, 10%, X7R, 0603	TDK	C0603
1	C303	C2012X7S2A105K125AB	1 μ F/100 V	Capacitor, ceramic, 1 μ F, 100 V, 10%, X7S, 0805	TDK	C0805
1	C304	C1005C0G1H391K050BA	390 pF/50 V	Capacitor, ceramic, 390 pF, 50 V, 10%, NP0, 0402	TDK	C0402
4	C307, C308, C501, C504	C2012X7R1E475K125AB	4.7 μ F/25 V	Capacitor, ceramic, 4.7 μ F, 25 V, 10%, X7R, 0805	TDK	C0805
2	C401, C403	GRM32ER71A476ME15L	47 μ F/10 V	Capacitor, ceramic, 47 μ F, 10 V, 20%, X7R, 1210	Murata	C1210
1	C404	C1608X7R1H222M	2.2 nF/50 V	Capacitor, ceramic, 2200 pF, 50 V, 20%, X7R, 0603	TDK	C0603
1	C405	C1608X7R1H103M080AA	10 nF/50 V	Capacitor, ceramic, 10000 pF, 50 V, 20%, X7R, 0603	TDK	C0603
2	C406, C407	GRM31CR71A226KE15L	22 μ F/10 V	Capacitor, ceramic, 22 μ F, 10 V, 10%, X7R, 1206	Murata	C1206
1	C503	C1005X7S0J105K050BC	1 μ F/6.3 V	Capacitor, ceramic, 1 μ F, 6.3 V, 10%, X7S, 0402	TDK	C0402
2	C506, C507	C1005X7S1A105K050BC	1 μ F/10 V	Capacitor, ceramic, 1 μ F, 10 V, 10%, X7S, 0402	TDK	C0402
5	D102, D201, D202, D204, D501	BAS516_115	BAS516	Diode switch, 100 V, 0.25 A, SOD523	NXP	SOD523as
1	D203	ZR431F01TA	ZR431	IC VREF shunt precision adjustable SOT-23	DIODES	SOT23
1	D401	PD3S160-7	PD3S160-7	Diode Schottky, 60 V, 1 A, POWERDI323	DIODES	powerdi323as
1	JP1		VIN+	Swage Terminal Pin 1.0 mm		
1	JP2		ON/OFF	Swage Terminal Pin 1.0 mm		
1	JP3		VIN-	Swage Terminal Pin 1.0 mm		
1	JP4		VOUT+	Swage Terminal Pin 1.5 mm		
1	JP5		VSENSE+	Swage Terminal Pin 1.0 mm		
1	JP6		NC	Swage Terminal Pin 1.0 mm		
1	JP7		VSENSE-	Swage Terminal Pin 1.0 mm		
1	JP8		VOUT-	Swage Terminal Pin 1.5 mm		
1	JP10	NRPN071PAEN-RC	dosa	Connector header 2 mm single straight 7-position	Sullins	dosa7
1	L101	PIMB042T-R47MS	0.47 μ H	Power choke coil PIMB042T type	Cyntec	pimb042t
1	L401	RM6ILP	RM6ILP	Inductor RM6ILP	TDK	rm6ilp
2	Q101, Q102	BSC520N15NS3 G	BSC520	MOSFET, N-CH, 150 V, 21 A, TDSO-8	Infineon	PWRPAKSO8
1	Q103	SI7115DN-T1-E3	SI7115	MOSFET, P-CH, D-S, 150 V, PPAK 1212-8	Vishay Siliconix	PPAK1212_8
1	Q201	BC846BM3T5G	BC846BM3T5G	Transistor, NPN, 65 V, 100 mA, SOT-723	ON Semi	SOT723
1	Q202	MMBT2907AWT1G	MMBT2907	Transistor, GP SS PNP, 60 V, SOT323	ON Semi	SOT323
1	Q401	BSC010N04LSI	BSC010N04LSI	MOSFET, N-CH, 40 V, 100 A, TDSO-8	Infineon	PWRPAKSO8
2	Q402, Q403	SIR662DP-T1-GE3	SIR662DP	MOSFET, N-CH, 60 V, 60 A, 8-SO PWRPAK	Fairchild	PWRPAKSO8
1	RT1	NCP15WF104F03RC	100 k Ω	Thermistor, 100 k Ω , NTC 0402 SMD	Vishay Dale	R0402

Qty	Ref	Part Number	Value	Description	Vendor	Package
1	R105	CRCW06034R70FKEA	4.7 Ω	Resistor, 4.70 Ω , 1/10 W, 1%, 0603 SMD	Vishay Dale	R0603
10	R106, R107, R204, R205, R215, R218, R233, R311, R401, R403	CRCW040210K0FKED	10 k Ω	Resistor, 10.0 k Ω , 1/16 W, 1%, 0402 SMD	Vishay Dale	R0402
5	R203, R225, R234, R237, R238	CRCW04025K11FKED	5.11 Ω	Resistor, 5.11 k Ω , 1/16 W, 1%, 0402 SMD	Vishay Dale	R0402
1	R206	CRCW060320R0FKEA	20 Ω	Resistor, 20.0 Ω , 1/10 W, 1%, 0603 SMD	Vishay Dale	R0603
2	R208, R304	CRCW0402680RFKED	680 Ω	Resistor, 680 Ω , 1/16 W, 1%, 0402 SMD	Vishay Dale	R0402
1	R209	CRCW040218K2FKED	18.2 k Ω	Resistor, 18.2 k Ω , 1/16 W, 1%, 0402 SMD	Vishay Dale	R0402
1	R210	CRCW04021K50FKED	1.5 k Ω	Resistor, 1.50 k Ω , 1/16 W, 1%, 0402 SMD	Vishay Dale	R0402
1	R211	CRCW040222K6FKED	22.6 k Ω	Resistor, 22.6 k Ω , 1/16 W, 1%, 0402 SMD	Vishay Dale	R0402
1	R213	CRCW04021K00FKED	1 k Ω	Resistor, 1.00 k Ω , 1/16 W, 1%, 0402 SMD	Vishay Dale	R0402
1	R214	CRCW040216K5FKED	16.5 k Ω	Resistor, 16.5 k Ω , 1/16 W, 1%, 0402 SMD	Vishay Dale	R0402
2	R216, R219	CRCW04022K00FKED	2 k Ω	Resistor, 2.00 k Ω , 1/16 W, 1%, 0402 SMD	Vishay Dale	R0402
1	R217	CRCW040210R0FKED	10 Ω	Resistor, 10.0 Ω , 1/16 W, 1%, 0402 SMD	Vishay Dale	R0402
1	R221	Open	Open	Resistor, 2.20 k Ω , 1/16 W, 1%, 0402 SMD	Vishay Dale	R0402
2	R222, R224	CRCW04022K20FKED	2.2 k Ω	Resistor, 2.20 k Ω , 1/16 W, 1%, 0402 SMD	Vishay Dale	R0402
1	R226	TNPW040210K0BEED	10 k Ω , 0.1%	Resistor, 10.0 k Ω , 1/16 W, 0.1%, 0402	Vishay Dale	R0402
1	R227	CRCW0402100RFKED	100 Ω	Resistor, 100 Ω , 1/16 W, 1%, 0402 SMD	Vishay Dale	R0402
3	R231, R239, R303	CRCW040249K9FKED	49.9 k Ω	Resistor, 49.9 k Ω , 1/16 W, 1%, 0402 SMD	Vishay Dale	R0402
1	R232	CRCW0402200KFKED	200 k Ω	Resistor, 200 k Ω , 1/16 W, 1%, 0402 SMD	Vishay Dale	R0402
1	R235	CRCW04028K20FKED	8.2 k Ω	Resistor, 8.20 k Ω , 1/16 W, 1%, 0402 SMD	Vishay Dale	R0402
1	R236	CRCW040251K1FKED	51.1 k Ω	Resistor, 51.1 k Ω , 1/16 W, 1%, 0402 SMD	Vishay Dale	R0402
2	R301, R302	CRCW0402374KFKED	374 k Ω	Resistor, 374 k Ω , 1/16 W, 1%, 0402 SMD	Vishay Dale	R0402
1	R309	CRCW040220K5FKED	20.5 k Ω	Resistor, 20.5 k Ω , 1/16 W, 1%, 0402 SMD	Vishay Dale	R0402
1	R310	CRCW04026K81FKED	6.81 k Ω	Resistor, 6.81 k Ω , 1/16 W, 1%, 0402 SMD	Vishay Dale	R0402
2	R402, R407	CRCW06035R11FKEA	5.11 Ω	Resistor, 5.11 Ω , 1/10 W, 1%, 0603 SMD	Vishay Dale	R0603
3	R404, R405, R406	CRCW06035K11FKEA	5.11 k Ω	Resistor, 5.11 k Ω , 1/10 W, 1%, 0603 SMD	Vishay Dale	R0603
1	T1	Transformer	RM7ILP	Transformer RM7ILP	TDK	rm7ilp
1	T10	CST7030_100L	CT	SMT current sense transformer EE4.2	Coilcraft	cst7030
1	T12	SG0522_AE	SG0522	Flyback/buck transformer	Coilcraft	SG0522
1	U201	PS2911-1-V-F3-M-A	PS2911	Optocoupler trans 2.5 kV RMS 4SMD	CEL	MSOP4
1	U301	UCC25230DRMT	UCC25230	IC reg multi config sync 8 VSON	TI	DFN8
1	U501	ADUM3221ARZ-RL7	ADuM3221	IC DGTL ISO 2CH logic 1 MHZ 8SOIC	Analog Devices	R-8Z
1	U502	ADP3654ARHZ-RL	ADP3654	IC MOSFET DVR 4 A dual HS 8SOIC	Analog Devices	MSOP8_TP
1	U503	MIC5213-3.3YC5	MIC5213	IC REG LDO 3.3 V, 80 MA SC70-5	Micrel	SC70
1	U504	ADP1050	ADP1050	IC digital power management, 20-lead LFCSP	Analog Devices	LFCSP_20

NOTES



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS (\$100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.

©2014 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
UG12307-0-10/14(0)



www.analog.com