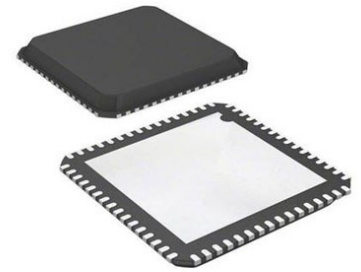


## LVDS Serializer 3675Mbps 1.2V Automotive 64-Pin VQFN EP T/R



Images are for reference only

[Inquiry](#)

**Manufacturer:** [Texas Instruments, Inc](#)

**Package/Case:** VQFN-64

**Product Type:** Drivers

**RoHS:** RoHS Compliant/Lead free 

**Lifecycle:** Active

### General Description

The DS90UB941AS-Q1 is a dual DSI to FPD-Link III bridge serializer designed for automotive infotainment applications. When paired with an FPD-Link III DS90UB940N-Q1, DS90UB948-Q1, DS90UB924-Q1, DS90UB926Q-Q1 or DS90UB928Q-Q1 deserializer, the DS90UB941AS-Q1 can supply 1- or 2-lane high-speed serial streams over cost-effective, 50  $\Omega$ , single-ended coaxial cables or over 100  $\Omega$ , differential shielded twisted-pair (STP) and shielded twisted-quad (STQ) cables. In response to the rise in number and variance of displays in infotainment systems, the DS90UB941AS-Q1 can support symmetric and asymmetric splitting.

The DS90UB941AS-Q1 can consolidate video data over two differential pairs to simplify system design and decrease the interconnect size and weight of the application.

The FPD-Link III interface supports video and audio data transmission and full duplex control, including I2C communication and up to eight I2S audio channels over the same high-speed serial link. EMI is minimized by the use of low voltage differential signaling, data scrambling, and randomization.

## Key Features

AEC-Q100 qualified for automotive applications with the following results:

Device temperature grade 2: 40°C to +105°C ambient operating temperature

Supports pixel clock frequency up to 210 MHz for 3K (2880x1620) at 30Hz, QXGA (2048x1536), 2K (2880x1080), WUXGA (1920x1200), or 1080p60 (1920x1080) resolutions with 24-bit color depth

MIPI D-PHY / Display Serial Interface (DSI) receiver provides a high-bandwidth interface to video processor or FPGA

Dual DSI input ports with up to 4 data lanes each

Up to 1.5 Gbps per lane

Superframe with symmetric and asymmetric unpacking capability

ECC and CRC generation

Virtual channel capability

Single and dual FPD-Link III outputs

Single link: up to 105MHz pixel clock

Dual link: up to 210MHz pixel clock

Functional Safety-Capable

Documentation available to aid ISO 26262 system design

Symmetric and asymmetric video splitting

## Recommended For You

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### SN65LVDS3486D

Texas Instruments, Inc

SOP-16

### SN65LVDS3487D

Texas Instruments, Inc

SOP16

### DS90C032TM

Texas Instruments, Inc

SOP16

### DS90C031BTM

Texas Instruments, Inc

SOP16

### SN65LVDS31PW

Texas Instruments, Inc

TSSOP-16

### SN65LVDS33D

Texas Instruments, Inc

SOP-16

### SN65LVDS32D

Texas Instruments, Inc

SOP-16

### SN65LVDS31D

Texas Instruments, Inc

SOP

### SN65LVDS32PW

Texas Instruments, Inc

TSSOP16

### DS90UB954TRGZIQ1

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QFN48

### DS90UB954TRGZRQ1

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VQFN48

### SN65DSI83TPAPRQ1

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HTQFP-64

**DS90UB947TRGCTQ1**

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VQFN-64

**DS90LV011AQMF/NOPB**

Texas Instruments, Inc

SOT23-5

**DS90UB924TRHSTQ1**

Texas Instruments, Inc

WQFN-48