
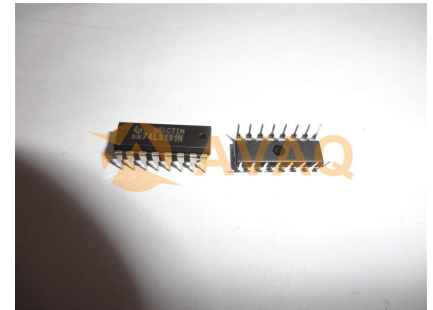


Counter Single 4-Bit Async Binary UP/Down 16-Pin PDIP Tube

Manufacturer:	Texas Instruments, Inc
Package/Case:	DIP16
Product Type:	Logic ICs
RoHS:	RoHS Compliant/Lead free 
Lifecycle:	Active



Images are for reference only

[Inquiry](#)

General Description

The '190, 'LS190, '191, and 'LS191 are synchronous, reversible up/down counters having a complexity of 58 equivalent gates. The '191 and 'LS191 are 4-bit binary counters and the '190 and 'LS190 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter count up and when high, it counts down. A false clock may occur if the down/up input changes while the clock is low. A false ripple carry may occur if both the clock and enable are low and the down/up input is high during a load pulse.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Series 54' and 54LS' are characterized for operation over the full military temperature range of -55°C to 125°C; Series 74' and 74LS' are characterized for operation from 0°C to 70°C.

Key Features

Counts 8-4-2-1 BCD or Binary

Single Down/Up Count Control Line

Count Enable Control Input

Ripple Clock Output for Cascading

Asynchronously Presetable with Load Control

Parallel Outputs

Cascadable for n-Bit Applications

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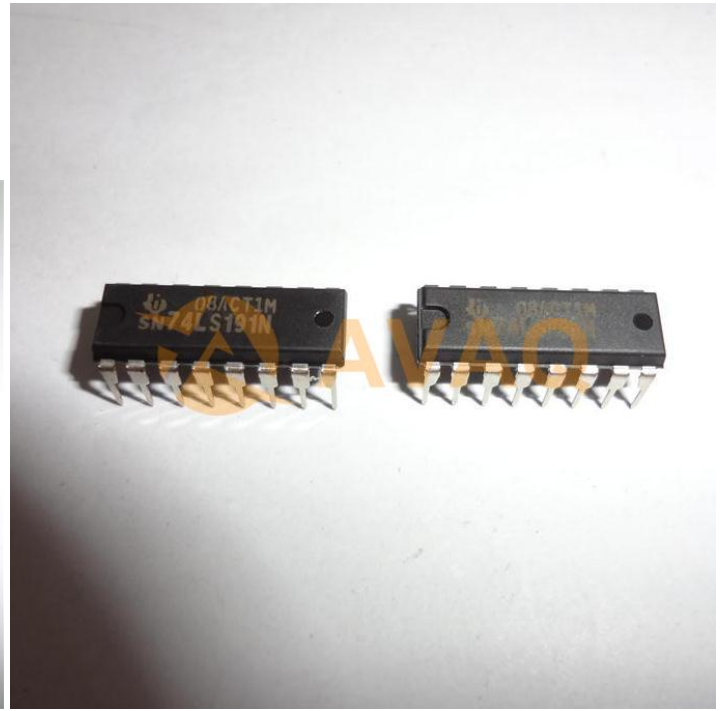
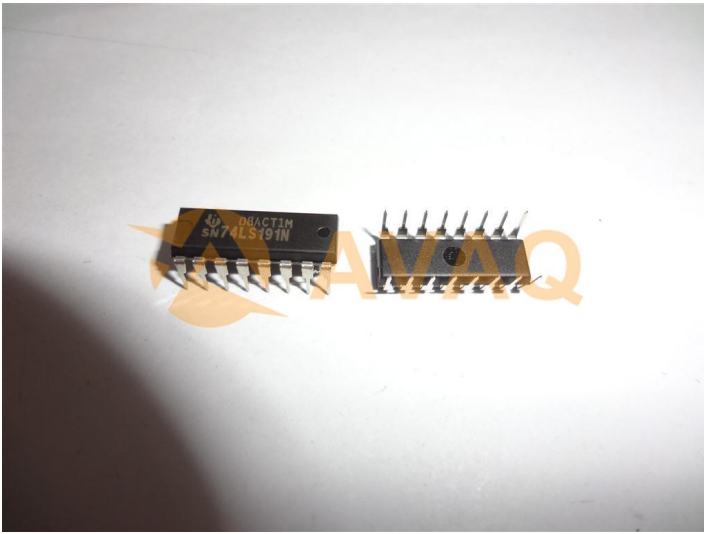
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Recommended For You

SN74HC191N

Texas Instruments, Inc

DIP

SN74LS293N

Texas Instruments, Inc

DIP14

SN74LS90N

Texas Instruments, Inc

DIP14

SN74LS93N

Texas Instruments, Inc

DIP

SN74LS590N

Texas Instruments, Inc

DIP

SN74HC4040N

Texas Instruments, Inc

DIP16

SN54HC193J

Texas Instruments, Inc

CDIP

SN74HC590AD

Texas Instruments, Inc

SOIC-16

SN74HC163D

Texas Instruments, Inc

SOP

SN74LS163AN

Texas Instruments, Inc

DIP

SN74LS161AN

Texas Instruments, Inc

DIP16

SN74F163AN

Texas Instruments, Inc

DIP16

SN74LV8154N

Texas Instruments, Inc

DIP-20

SN74LS393N

Texas Instruments, Inc

DIP

SN74HC590AN

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DIP16