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High-Efficiency
255 W ATX Power Supply
Reference Design
Documentation Package

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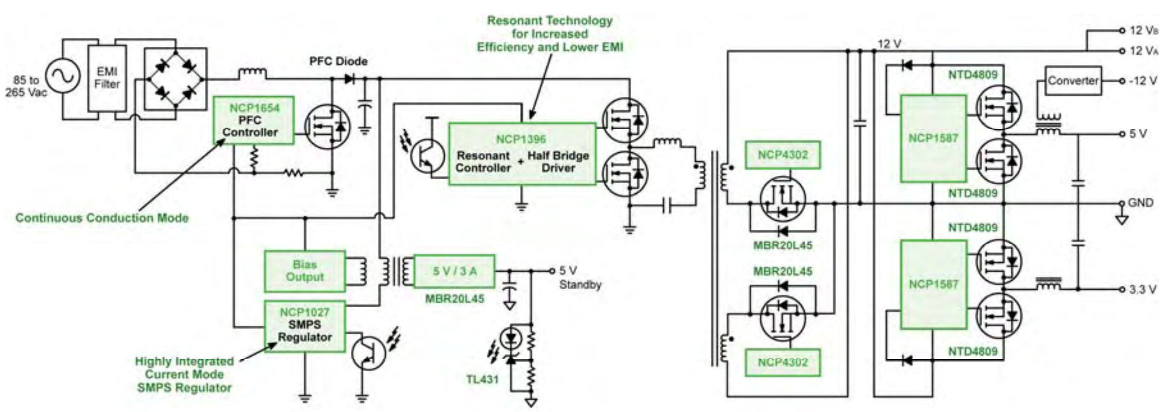
1. Overview

ON Semiconductor was the first semiconductor company to provide an 80 PLUS-certified open reference design for an ATX power supply in 2005. A second generation 80 PLUS-certified open reference design with improved efficiency was then introduced in 2007. ON Semiconductor is now introducing its third generation 80 PLUS-certified open reference design with a drastic efficiency improvement. This is a 255 W multi-output power supply for the ATX form factor. Achieving a maximum efficiency of 90% at 50% load, and at 230 and 240 Vac, this third generation reference design achieves >88% efficiency at 50% load, and 100 and 115 Vac. All efficiency measurements were obtained at the end of a 41 cm (16 in.) cable, ensuring the design can be used ‘as is’ in all standard desktop PC configurations.

This reference document provides the details behind this third generation design. The design manual provides a detailed view of the performance achieved with this design in terms of efficiency, performance, thermals and other key parameters. In addition, a detailed list of the bill-of-materials (BOM) is also provided. ON Semiconductor will also be able to provide technical support to help our customers design and manufacture a similar ATX power supply customized to meet their specific requirements.

The results achieved in this third generation design were possible due to the use of advanced new components from ON Semiconductor. These new ICs not only speeded up the overall development cycle for this new design, but also helped achieve the high efficiencies while at the same time keeping a check on the overall cost.

This third generation design consists of a single PCB designed to fit into the standard ATX enclosure along with a fan. Figure 1 below presents the overall architecture employed in this design. Detailed schematics are included later in this design manual.



Specification	20% load	50% load	100% load
• Multiple-Output • Non-Redundant • PFC 0.9 at 50%	85%	88%	85%

Figure 1: Reference Design Architecture Simplified Block Diagram

As seen in figure 1, the first stage, active Power Factor Correction (PFC) stage, is built around ON Semiconductor's Continuous Conduction Mode (CCM) PFC controller, NCP1654. The NCP1654 provides an integrated, robust and cost-effective PFC solution. The second stage features a resonant half-bridge LLC topology using ON Semiconductor's controller, NCP1396. This topology ensures maximum efficiency and minimizes EMI. The NCP1027, standby controller, is used to generate the 5 V standby output. The NCP1027 is an optimized integrated circuit for the ATX power supply and incorporates a high-voltage MOSFET.

On the secondary side, this architecture uses a synchronous rectification scheme built around ON Semiconductor's NCP4302 controller in order to generate a 12 V output. Finally, two identical DC-DC controllers are used to down-convert the 12 V into +5 V, +3.3 V and -12 V. The DC-DC controller is the NCP1587, a low voltage synchronous buck controller in a very small surface mount 8-pin package. Each DC-DC controller drives two NTD4809 (30 V, 58 A, single N-channel power MOSFET) in a synchronous rectification scheme.

With the introduction of this third generation, high-efficiency ATX Power Supply, ON Semiconductor has shown that with judicious choice of design tradeoffs, optimum performance is achieved at minimum cost.

2. Specifications

The design closely follows the ATX12V version 2.2 power supply guidelines and specifications available from www.formfactors.org, unless otherwise noted. This 255 W reference design exceeds the 80 PLUS Silver (www.80plus.org), ENERGY STAR® 5.0 (www.energystar.gov), and Climate Savers Computing Initiative (CSCI) Step 3 (www.climatesaverscomputing.org) efficiency targets for desktop PC multi-output power supplies. Table 1 hereafter shows a summary of the efficiency targets from these different organizations.

	Levels	Specification	20% of rated output	50% of rated output	100% of rated output	Compliance
Multi-Output ATX Power Supplies	80 PLUS	• Multiple-Output • Non-Redundant • PFC 0.9 at 100% of rated output	80% efficiency	80% efficiency	80% efficiency	ENERGY STAR rev. 4.0 & CSCI step #1 Effective date: July 2007
	80 PLUS BRONZE	• Multiple-Output • Non-Redundant • PFC 0.9 at 50% of rated output	82% efficiency	85% efficiency	82% efficiency	ENERGY STAR rev. 5.0 (Effective date: July 2009) & CSCI step #2 (June 2008 thru July 2009)
	80 PLUS SILVER	• Multiple-Output • Non-Redundant • PFC 0.9 at 50% of rated output	85% efficiency	88% efficiency	85% efficiency	CSCI step #3 (July 2009 thru June 2010)
	80 PLUS GOLD	• Multiple-Output • Non-Redundant • PFC 0.9 at 50% of rated output	87% efficiency	90% efficiency	87% efficiency	CSCI step #4 (July 2010 thru June 2011)

Table 1: Summary of Efficiency Targets

Key specifications for this reference design are included in Table below.

Input			Output Voltage (V_{dc})	DC Output Current		
Voltage (V_{ac})		Frequency (H_Z)		Min DC Current (A)	Full Load DC Current (A)	Max DC Current (A)
Min.	90	47	**+12 V_A**	0	9.50	13.0
Typ.	100	50	**+12 V_B**	0	5.12	7.0
	115	60	**+5 V**	0.3	9.44	15.0
	230	50	**+3.3 V**	0.3	5.03	8.0
	240	50	**-12 V**	0	0.32	0.4
Max.	264	63	**+5 V_{SB}**	0	2.39	3.0

Output Voltage (V_{dc})	Full Load DC Current (A)	Output Power	
		Full Load Output Power (W)	Notes
+12 V_A	9.50	114.0	Peak +12 V_{Adc} output current up to 14 A. Peak +12 V_{Bdc} output current to be 8 A. The maximum combined load on the +12 V_{Adc} and +12 V_{Bdc} outputs shall not exceed 220 W.
+12 V_B	5.12	61.4	
+5 V	9.44	47.2	The maximum continuous combined load on the +5Vdc and +3.3 Vdc outputs shall not exceed 80 W.
+3.3 V	5.03	16.6	
-12 V	0.32	3.8	
+5 V_{SB}	2.39	11.95	
		Full Load Total Output Power = 255 W	

Output Voltage (V_{dc})	Output Voltage Regulation (V)			Tolerance (%)	Output Ripple / Noise (mVpp)
	Min.	Typ.	Max.		
+12 V_A	+11.4	+12	+12.6	±5	120
+12 V_B	+11.4	+12	+12.6	±5	120
+5 V	+4.75	+5	+5.25	±5	70
+3.3 V	+3.14	+3.3	+3.47	±5	50
-12 V	-10.8	-12	-13.2	±10	250
+5 V_{SB}	+4.75	+5	+5.25	±5	100

Table 2: Target Specifications

Target specifications for other key parameters of the reference design include:

- Efficiency: Minimum efficiency of 85% at 20% and at 100% of rated output power, and 88% at 50% of rated output power as defined by the 80 PLUS requirements.
- Power Factor: Power factor of 0.9 or greater at 100 % load.
- Input Voltage: Universal Mains: 90 Vac to 265 Vac, frequency: 47 to 63 Hz.
- Safety Features: As per the ATX12V version 2.2 power supply guidelines, this design includes safety features such as OVP, UVP, and OCP.

3. Architecture Overview

The architecture selected is designed around a succession of conversion stages as illustrated in Figure 1. The first stage is a universal input, active power factor boost stage delivering a constant output voltage of 385 V to the second stage, the half bridge resonant LLC converter. On the secondary side, this architecture uses a synchronous rectification scheme built around ON Semiconductor's NCP4302 controller in order to generate a +12 V output. Finally, the +12 V is down-converted +5 V, +3.3 V and -12 V by a DC-DC conversion stage, built around two identical DC-DC controllers. In addition, a small integrated flyback converter delivers 12 W of standby power to another isolated 5 V rail. All the different voltage rails are monitored by a dedicated supervisory controller.

ON Semiconductor has developed multiple power management controllers and MOSFET devices in support of the ATX program. Web-downloadable data sheets, design tools and technical resources are available to assist design optimization. The semiconductor components, supporting the ATX Generation 3 platform, are the NCP1654 PFC controller, the NCP1396 half-bridge resonant LLC controller, the NCP4302 synchronous rectification, the NCP1027 standby controller, the NCP1587 DC-DC controller with synchronous rectification, and the NTD4809 single N-channel power MOSFET driven by the NCP1587, in synchronous rectification.

3.1 Primary Side: PFC Stage

There are a variety of PFC topologies available. These include discontinuous conduction mode (DCM), critical conduction mode (CRM) and continuous conduction mode (CCM). At this power level, CCM is the preferred choice and the NCP1654 will implement an IEC61000-3-2 compliant, fixed frequency, peak current mode or average current mode PFC boost converter with very few external components.

3.2 Primary Side: Half bridge resonant LLC Converter

The heart of the half-bridge resonant LLC converter stage is the NCP1396 resonant mode controller. Thanks to its proprietary high-voltage technology, this controller includes a bootstrapped MOSFET driver for half-bridge applications accepting bulk voltages up to 600 V. Protections featuring various reaction times, e.g. immediate shutdown or timer-based event, brown-out, broken optocoupler detection etc., contribute to a safer converter design, without engendering additional circuitry complexity. An adjustable dead-time also helps lower the shoot-through current contribution as the switching frequency increases. More information about LLC structure can be found in the ON Semiconductor application note AND8311/D (Understanding the LLC Structure in Resonant Applications).

3.3 Secondary Side: Synchronous Rectification

The 12 V output generated by the half-bridge resonant LLC converter is rectified using a proprietary synchronous rectification scheme built around two NCP4302 and two external single N-channel MOSFETs.

3.4 Secondary Side: DC-DC Conversion Stage

Two identical DC-DC controllers are used to down-convert the 12 V into +5 V and +3.3 V. The DC-DC controller is the NCP1587, a low voltage synchronous buck controller in a very small surface mount 8-pin package. The NCP1587 is a low cost PWM controllers designed to operate from a 5 V or 12 V supply. This device is capable of producing an output voltage as low as 0.8 V. The NCP1587 provides a 1 A gate driver design and an internally set 275 kHz (NCP1587) oscillator. Other efficiency enhancing features of the gate driver include adaptive non overlap circuitry. The NCP1587 also incorporates an externally compensated error amplifier and a capacitor programmable soft start function. Protection features include programmable short circuit protection and under voltage lockout. Each DC-DC controller drives two NTD4809 (30 V, 58 A, single N-channel power MOSFET) in a synchronous rectification scheme.
The -12 V is generated from the +5 V using a small discrete-based converter.

3.5 Secondary Side: Monitoring and Supervisory Stage

The four dc outputs +5 V, +3.3 V, +12 V_A and +12 V_B are monitored by a dedicated monitoring controller which also provides over-current protection, over-voltage protection, under-voltage protection and generates the Power Good logic signal.

3.6 Standby Power

The NCP1027 integrates a fixed frequency current mode controller and a 700 volt MOSFET. The NCP1027 is an ideal part to implement a flyback topology delivering 15 W to an isolated 5 V output. At light loads the IC will operate in skip cycle mode, thereby reducing its switching losses and delivering high efficiency throughout the load range.

4. Performance Results

Measurements are done at three loading conditions, the load being expressed as a % of the rated output power, i.e. at 20%, 50% and at 100% of rated output power.
Measurements are also done at four AC line voltages, at 100 Vac, 115 Vac, 230 Vac and 240 Vac, at 50 Hz, 60 Hz and 63 Hz.
All measurements are taken at the end of the 41 cm-long (16 inches) cable.

The converter efficiency is measured according to the loading conditions detailed in Table 3:

Load as % of rated output power	**Output Current (A)**					
	+12V$_A$	**+12V$_B$**	**+5V**	**+3.3V**	**-12V**	**+5V$_{SB}$**
20%	1.90	1.02	1.89	1.01	0.06	0.48
50%	4.75	2.56	4.72	2.52	0.16	1.20
100%	9.50	5.12	9.44	5.03	0.32	2.39
Max.	13.0	7.0	15.0	8.0	0.4	3.0

Table 3: Load Matrix for Efficiency Measurements

4.1 Total Efficiency

	Total Efficiency (%)		
AC Input	**20% Load**	**50% Load**	**100% Load**
100 V$_{AC}$ / 50 H$_Z$	85.9%	88.3%	85.9%
115 V$_{AC}$ / 60 H$_Z$	86.3%	88.8%	86.8%
230 V$_{AC}$ / 50 H$_Z$	86.5%	90.1%	88.7%
240 V$_{AC}$ / 63 H$_Z$	86.5%	90.1%	88.8%

Table 4: Efficiency Results

The converter achieves over 85% efficiency with room to spare over all load conditions. All measurements are done at the end of the power cable.

4.2 Power Factor

The power factor exceeds 0.9 over all operating conditions as shown in Table .

	Power Factor			**Specification**
AC Input	**20% Load**	**50% Load**	**100% Load**	
100 V$_{AC}$ / 50 H$_Z$	0.96	0.983	0.987	PF > 0.90 @100% & 50% of rated output power
115 V$_{AC}$ / 60 H$_Z$	0.945	0.978	0.986	
230 V$_{AC}$ / 50 H$_Z$	0.714	0.912	0.966	
240 V$_{AC}$ / 63 H$_Z$	0.689	0.902	0.962	

Table 5: Power Factor vs Load as % of Rated Output Power

4.3 Standby Power

AC Input	Output Current on $+5V_{SB}$ (A)	Input Power (W)	Specification
100 V_{AC} / 50 H_Z	0.147	0.36	< 1W • U.S. Department of Energy, FEMP (Federal Energy Management Program): http://www1.eere.energy.gov/femp/procurement/index.html • Executive Order 13221 of July 31, 2001: http://www1.eere.energy.gov/femp/pdfs/eo13221.pdf
115 V_{AC} / 60 H_Z	0.171	0.31	
230 V_{AC} / 50 H_Z	0.244	0.55	
240 V_{AC} / 63 H_Z	0.312	0.57	

Table 6: Standby Power vs AC Line Voltage

4.4 Input Current

AC Input	Measurement (A)			Specification
	20% Load	50% Load	100% Load	
90 V_{AC} / 47 H_Z	0.673	1.609	3.245	90V (max 3.6A) 180V (max.1.8A) @ 100% load
100 V_{AC} / 50 H_Z	0.614	1.458	2.952	
115 V_{AC} / 63 H_Z	0.544	1.271	2.549	
180 V_{AC} / 50 H_Z	0.363	0.799	1.573	
230 V_{AC} / 53 H_Z	0.355	0.667	1.266	
240 V_{AC} / 60 H_Z	0.353	0.646	1.217	
264 V_{AC} / 63 H_Z	0.339	0.597	1.092	

Table 7: Input Current vs Load and AC Line Voltage

4.5 Inrush Current

Parameter Description	Min.	Typ.	Max.	Units
Initial In-rush Current			55	A (Peak)
Secondary In-rush Current			35	A (Peak)

Table 8: Inrush Current Specification

AC Input	Output Load	Measurement (A)		Specification
90 V_{AC}/47 H_Z	100% Load	Initial In-rush Current	9.9	Initial In-rush Current < 55 A Secondary In-rush Current < 35 A
		Secondary In-rush Current	8.0	
120 V_{AC}/63 H_Z	100% Load	Initial In-rush Current	17.9	
		Secondary In-rush Current	16.2	
220 V_{AC}/50 H_Z	100% Load	Initial In-rush Current	25.4	
		Secondary In-rush Current	24.5	
264 V_{AC}/63 H_Z	100% Load	Initial In-rush Current	34.1	
		Secondary In-rush Current	33.3	

Table 9: Inrush Current vs AC Line Voltage

4.6 Output Transient Response (Dynamic Loading)

Output Transient starting Load T1 / T2 (0.1 A/µsec), T1 / T2 (1 ms)

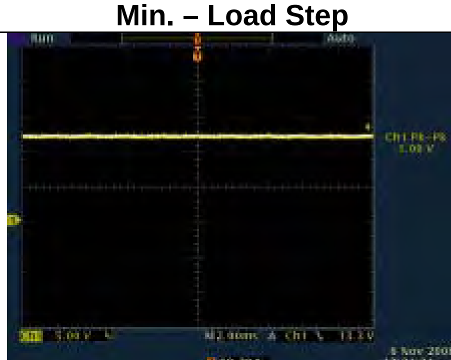
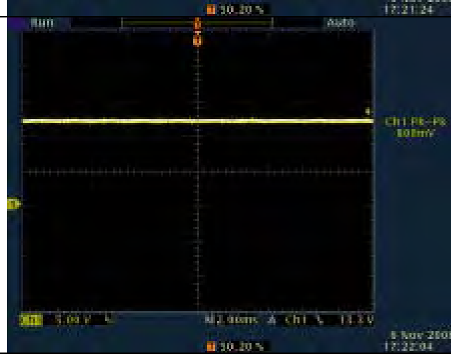
DC Output	Load (A)			Voltage Max. (V)	
	Min.	Load Step	Max.	Overshoot	Undershoot
+12 V_A	0.5	6.5	6.5	0.6	0.6
+12 V_B	0.5	3.5	3.5	0.6	0.6
+5 V	0.3	5	10	0.25	0.25
+3.3 V	0.3	2.66	5.34	0.17	0.17
-12 V	0	0.17	0.33	0.6	0.6
+5 V_{SB}	0	1.33	2.67	0.25	0.25

Table 10: Output Transient Response (Dynamic Loading)

4.7 Overshoot at Turn-On/Turn-Off

DC Output	Min. – Load Step	Load Step – Max.	Specification	Unit
+12V_A	0.34	N/A	1.2	V_{P-P}
+12V_B	0.38	N/A	1.2	
+5V	0.21	0.23	0.5	
+3.3V	0.15	0.17	0.33	
-12V	0.18	0.20	-1.2	
+5V_{SB}	0.21	0.20	0.5	

Table 11: Overshoot at Turn-On/Turn-Off

Measured and Calculated Data at 115V / 60H_Z		
DC Output	**Min. – Load Step**	**Load Step – Max.**
+12 V_A		N/A
+12 V_B		N/A

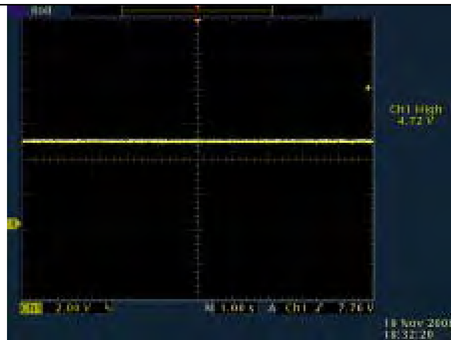
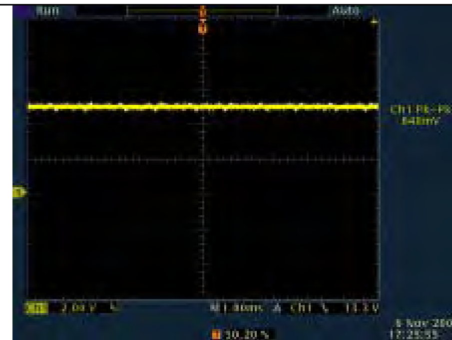
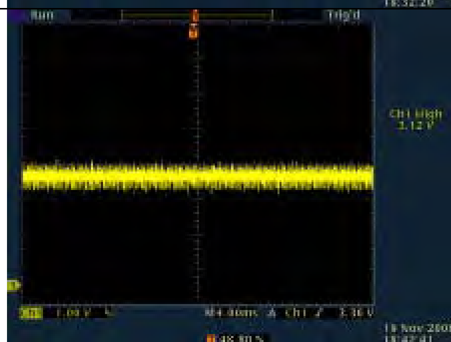
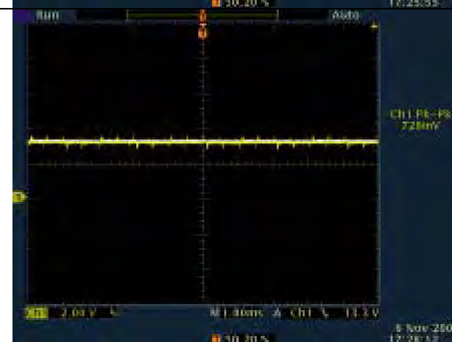
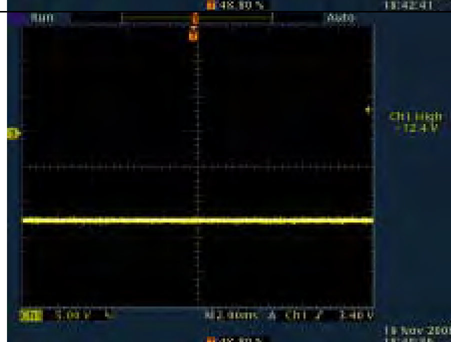
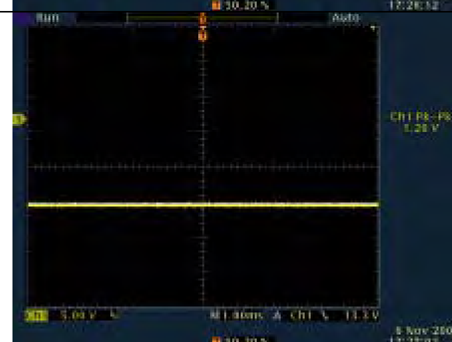
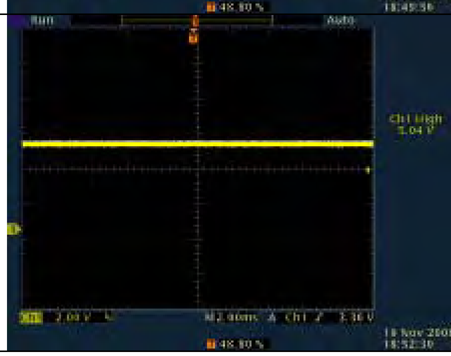
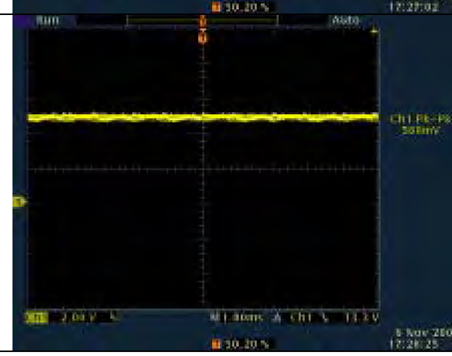
+5 V		
+3.3 V		
-12 V		
+5 V_{SB}		

Figure 2: Dynamic Load Test Waveforms

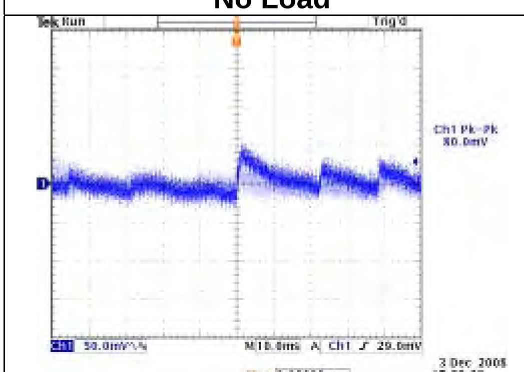
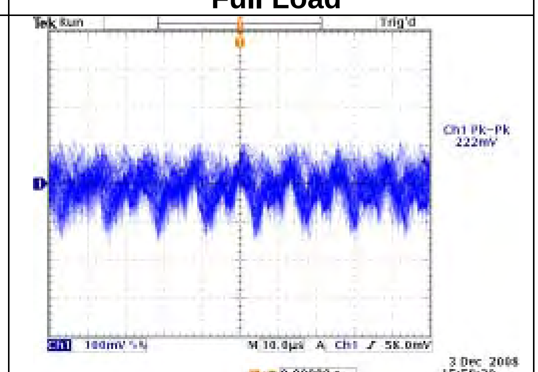
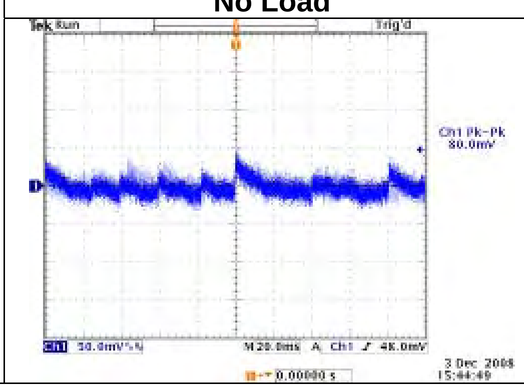
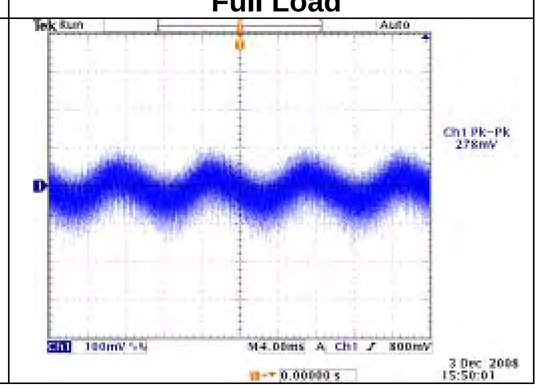
4.8 Output Ripple / Noise

The ripple voltage of each output is measured at no load and at the maximum load for each output., and at the four different line voltages. The output ripple is measured across 10 μF/MLC parallel 1000 μF low ESR/ESL termination capacitors. Figure 3 through 6 show the output voltage ripple measurements. All outputs meet the voltage ripple requirements.

DC Output	No Load (A)	Full Load (A)	Output Ripple / Noise Max (mVp-p)
+12 V_A	0	9.50	120
+12 V_B	0	5.12	120
+5 V	0	9.44	70
+3.3 V	0	5.03	50
-12 V	0	0.32	250
+5 V_{SB}	0	2.39	100

Table 12: Output Ripple / Noise Specification

4.8.1 100 V_{AC} / 50 H_Z - Ripple / Noise Test Waveform

	No Load	Full Load
+12 V_A		
+12 V_B		

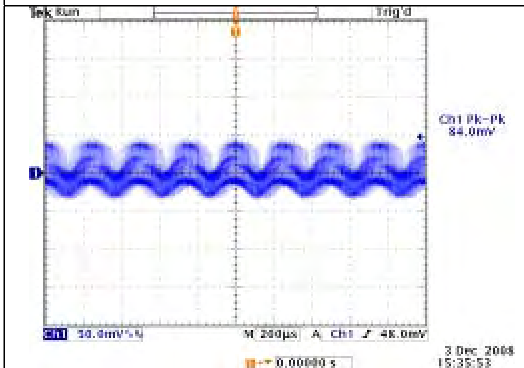
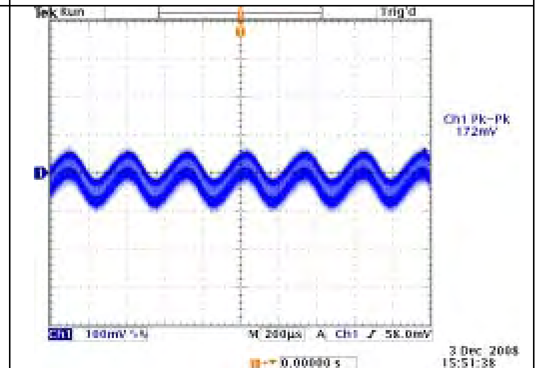
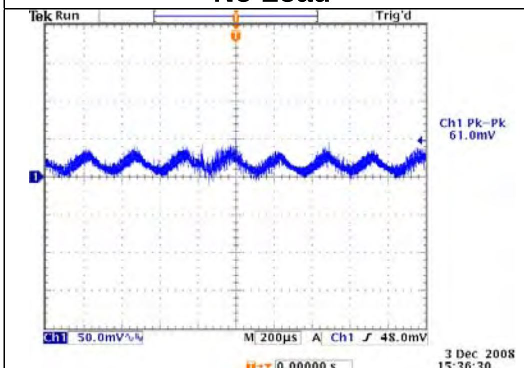
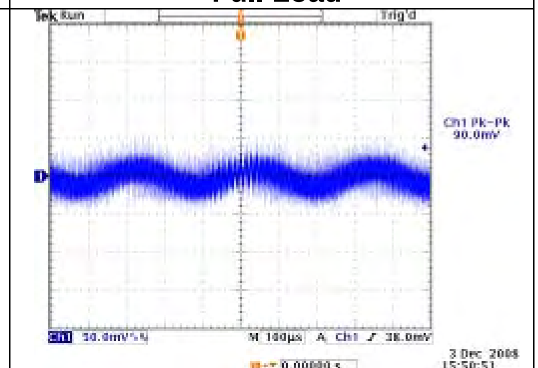
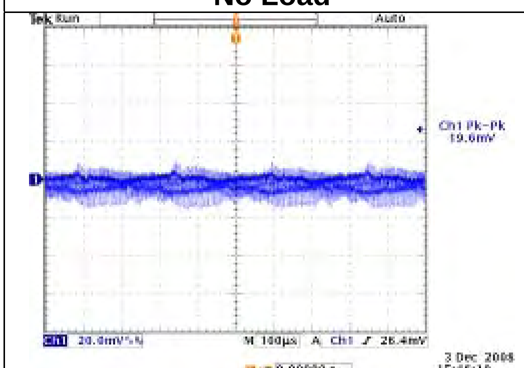
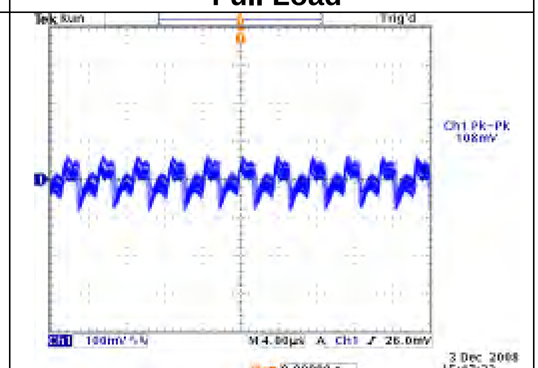
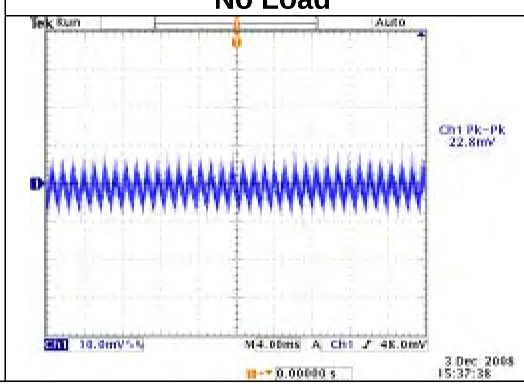
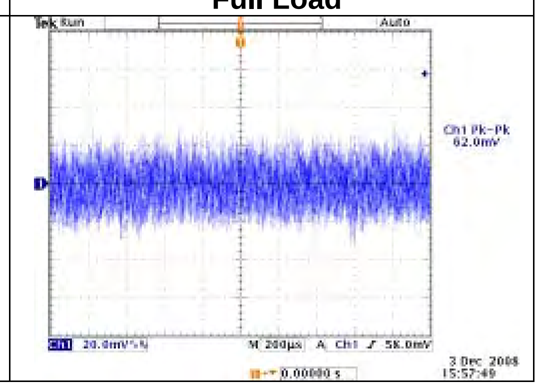
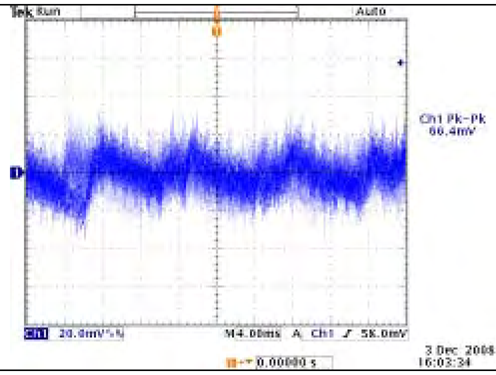
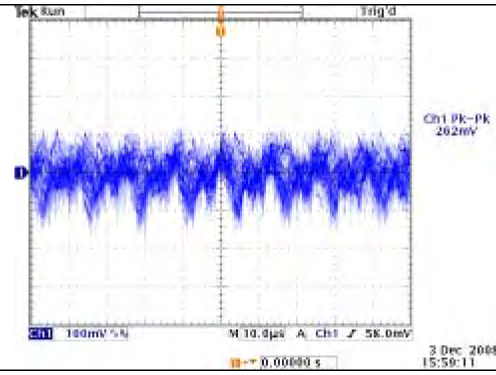
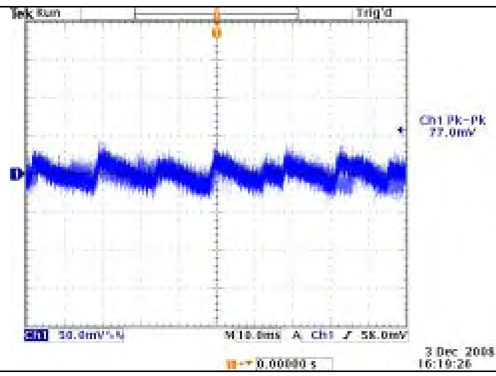
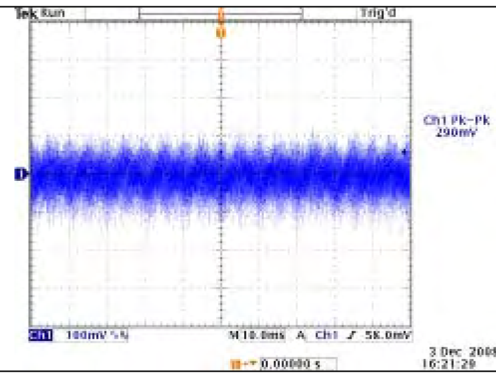
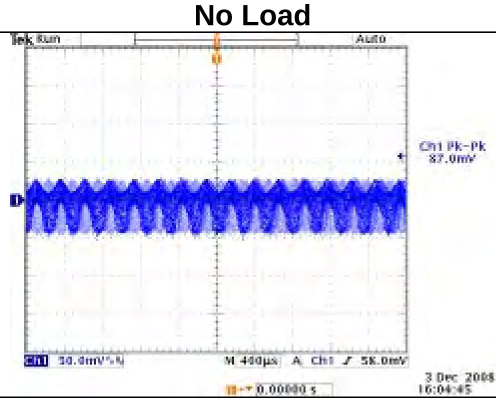
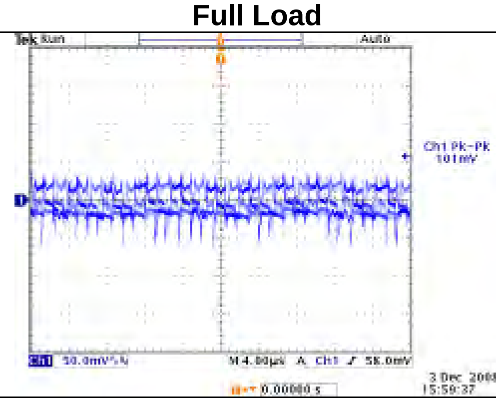
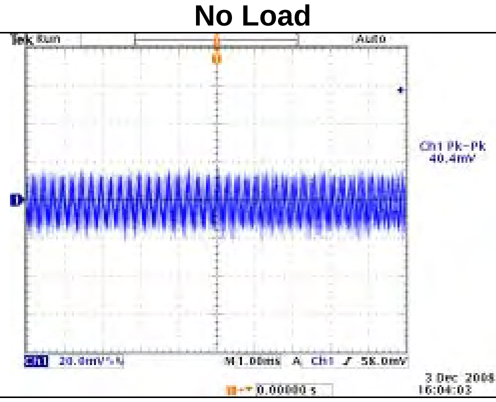
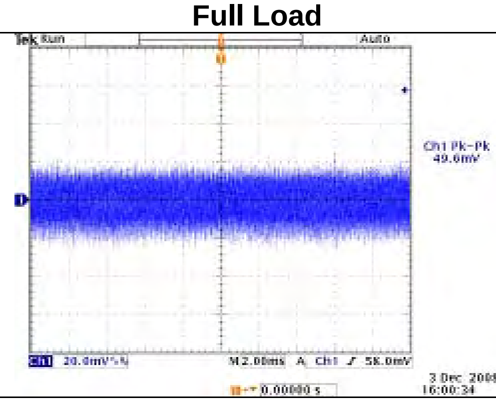
	No Load	Full Load
+5 V		
	No Load	**Full Load**
+3.3 V		
	No Load	**Full Load**
-12 V		
	No Load	**Full Load**
+5 V_{sB}		

Figure 3: ***100 V_{AC} / 50 H_Z - Ripple / Noise Test Waveform***

4.8.2 115 V_{AC} / 60 H_Z - Ripple / Noise Test Waveform

	No Load	Full Load
+12 V_A		
	No Load	**Full Load**
+12 V_B		
	No Load	**Full Load**
+5 V		
	No Load	**Full Load**
+3.3 V		

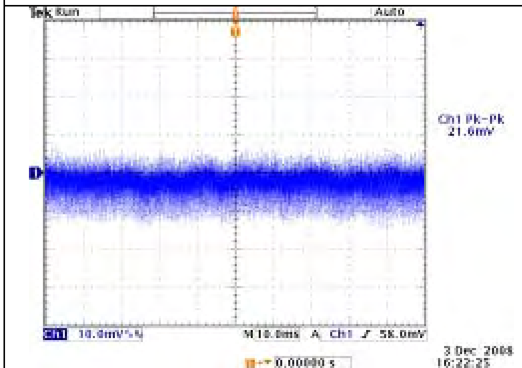
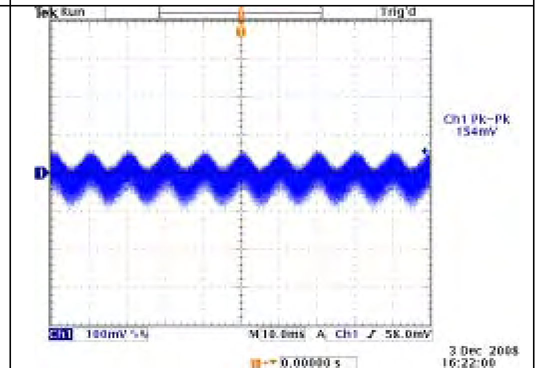
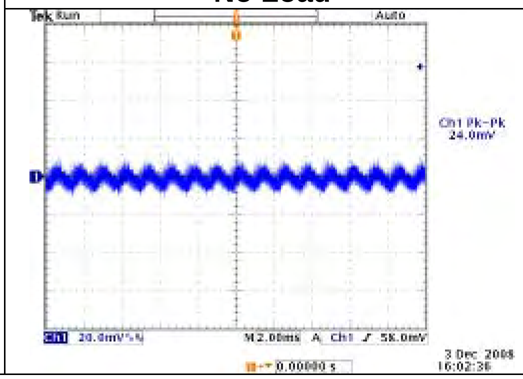
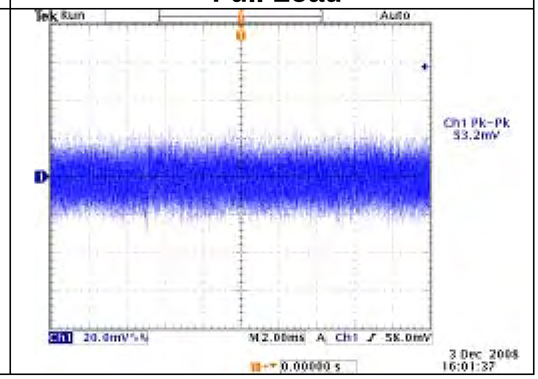
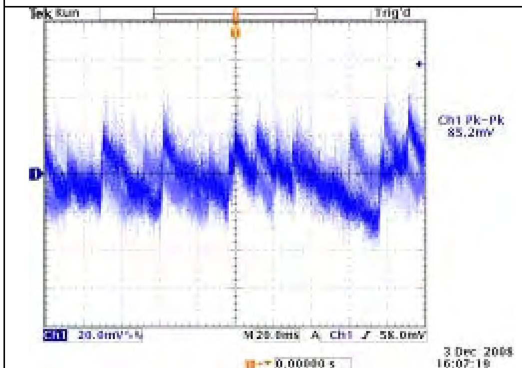
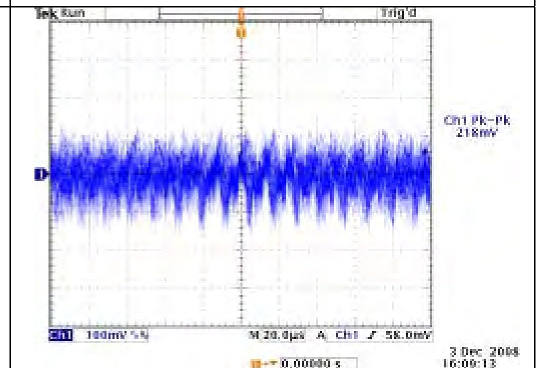
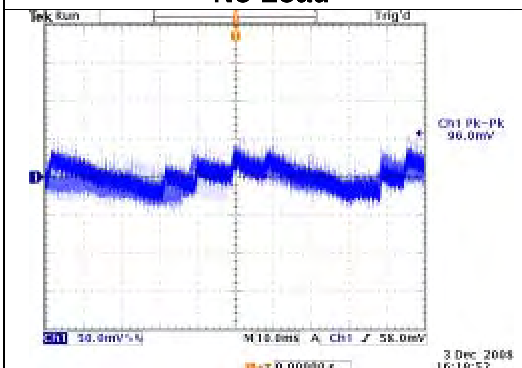
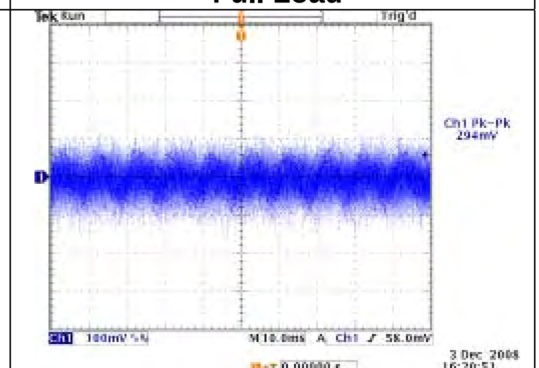
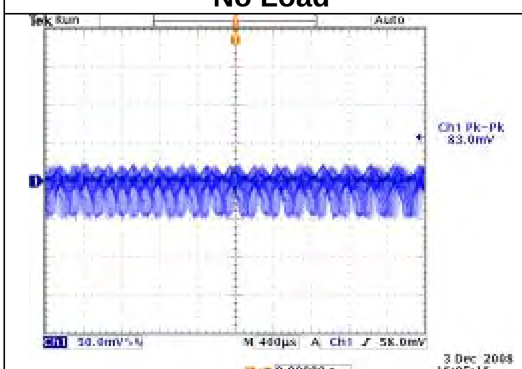
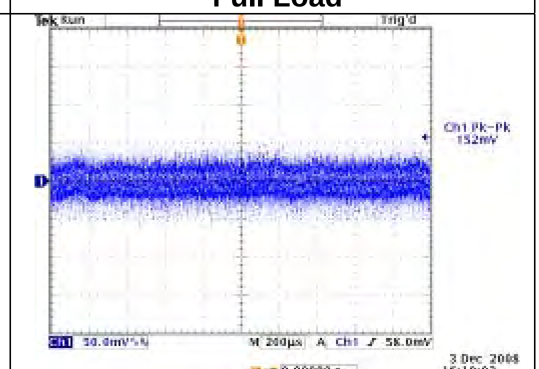
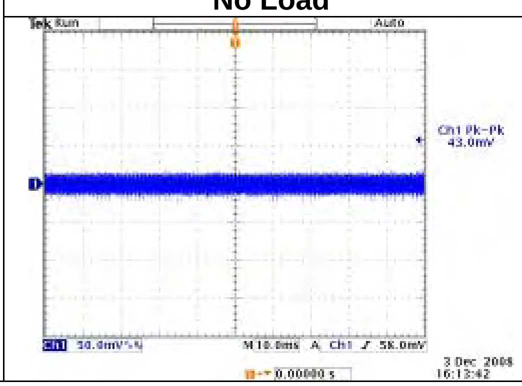
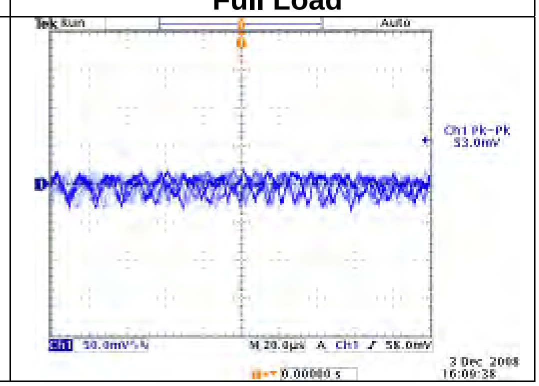
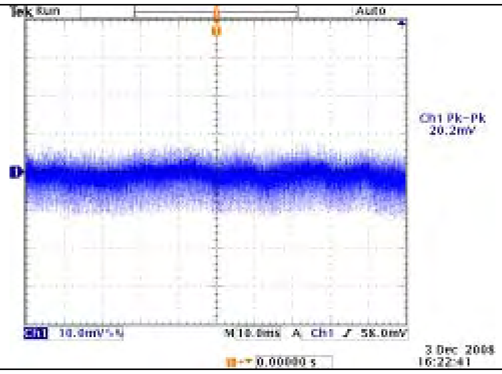
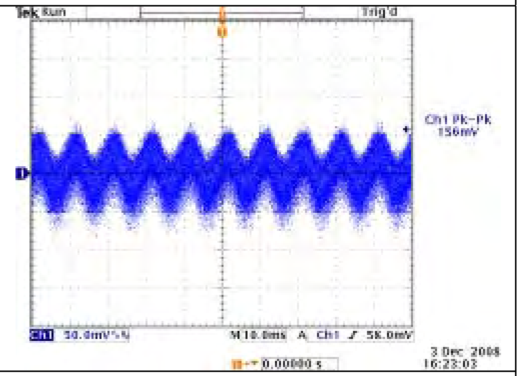
	No Load	Full Load
-12 V		
+5 V_{SB}		

Figure 4: ***115 V_{AC} / 60 H_Z - Ripple / Noise Test Waveform***

4.8.3 230 V_{AC} / 50 H_Z - Ripple / Noise Test Waveform

	No Load	Full Load
+12 V_A	 Ch1 Pk-Pk 85.2mV	 Ch1 Pk-Pk 218mV
+12 V_B	 Ch1 Pk-Pk 96.0mV	 Ch1 Pk-Pk 294mV
+5 V	 Ch1 Pk-Pk 83.0mV	 Ch1 Pk-Pk 152mV
+3.3 V	 Ch1 Pk-Pk 43.0mV	 Ch1 Pk-Pk 53.0mV

<table>
<tr><td rowspan="2">-12 V</td><td>No Load</td><td>Full Load</td></tr>
<tr><td>
</td><td>
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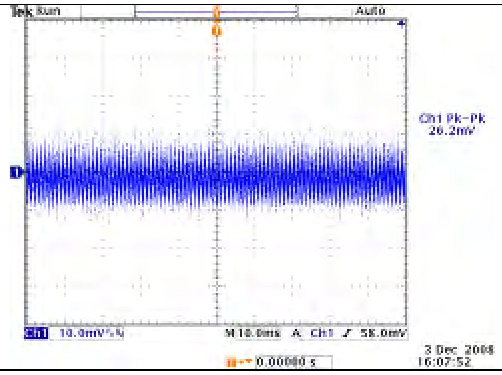
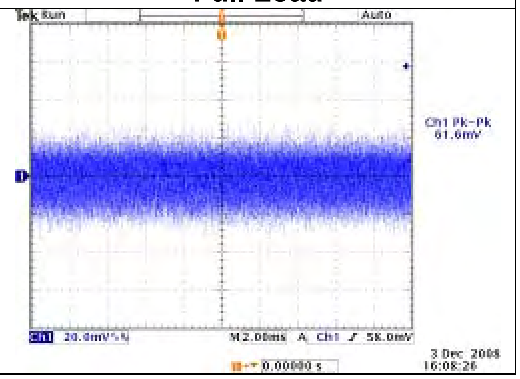
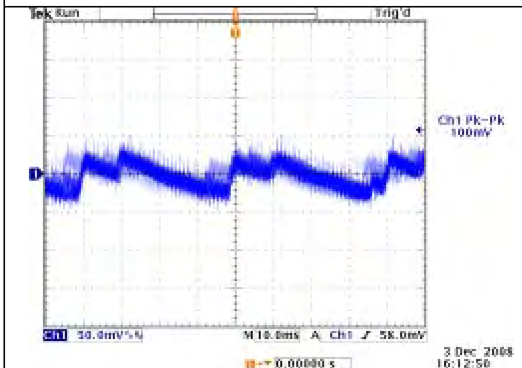
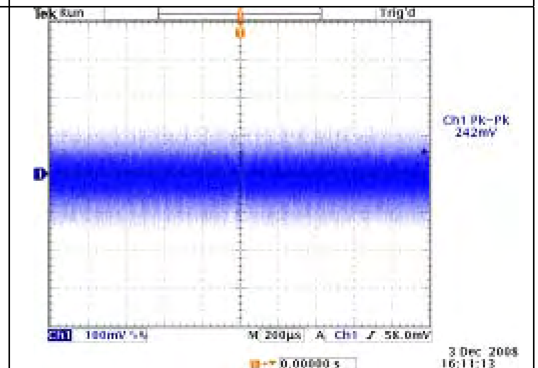
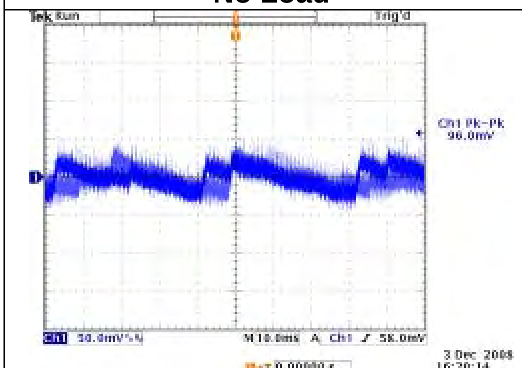
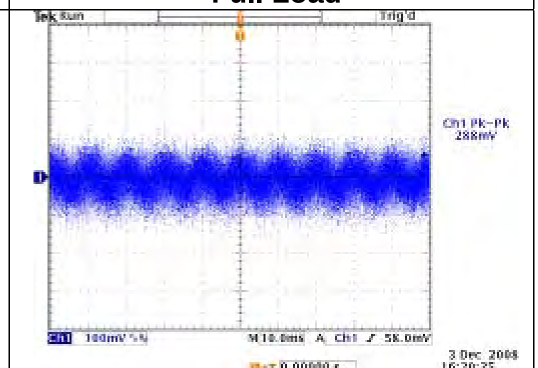
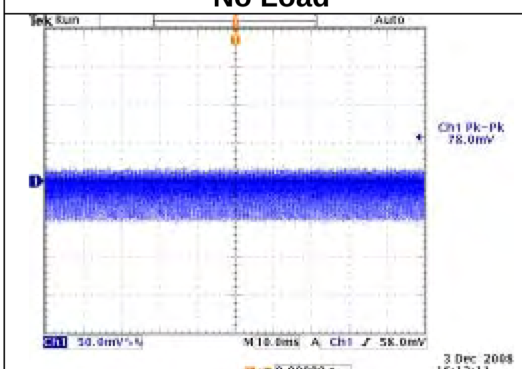
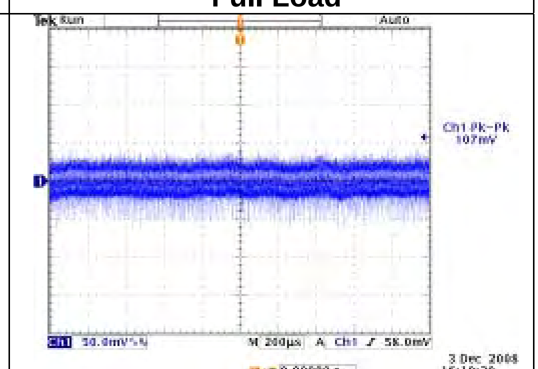
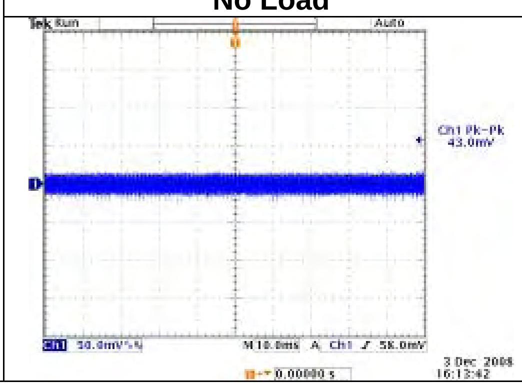
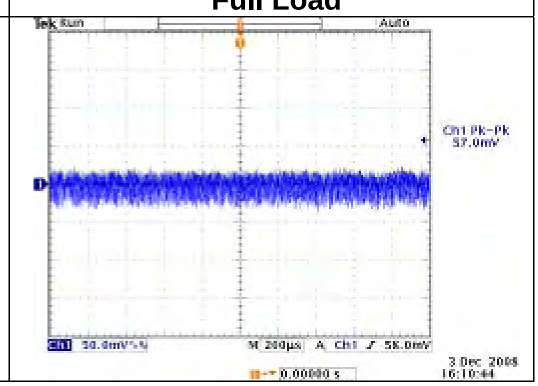
<tr><td rowspan="2">+5 V_{SB}</td><td>No Load</td><td>Full Load</td></tr>
<tr><td>
</td><td>
</td></tr>
</table>

Figure 5: ***230 V_{AC} / 50 H_Z - Ripple / Noise Test Waveform***

4.8.3 240 V_{AC} / 63 H_Z - Ripple / Noise Test Waveform

	No Load	Full Load
+12 V_A		
+12 V_B		
+5 V		
+3.3 V		

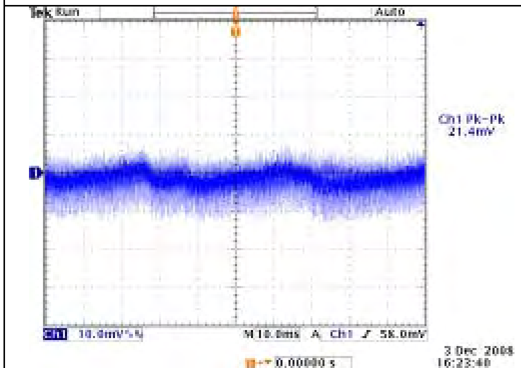
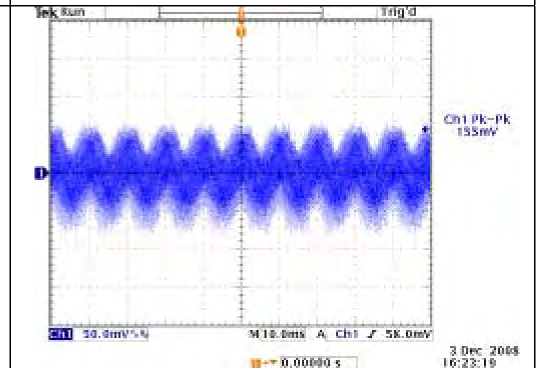
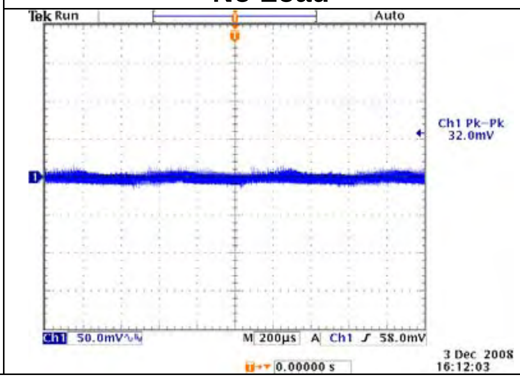
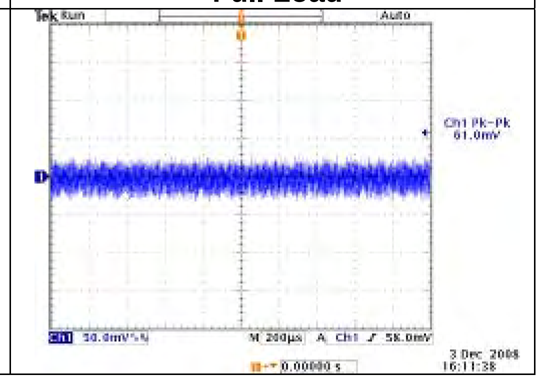
	No Load	Full Load
-12 V		
	No Load	**Full Load**
+5 V_{SB}		

Figure 6: ***240 V_{AC} / 63 H_Z - Ripple / Noise Test Waveform***

4.9 Hold-up Time

The required holdup time at 50% load is 16 ms. Holdup time is measured from the moment the AC power is removed to when the PWR_OK signal goes low. Figure 7 shows the holdup time at 50% load, and at 115 Vac and 230 Vac. Channel 4 is the AC power and Channel 1 is the PWR_OK signal.

AC Input	Dropout Loading Condition	Measurement (msec)	Specification
115 V_{AC} / 60 H_Z	50% Load	22	> 16 ms
230 V_{AC} / 50 H_Z	50% Load	23	

Table 13: Hold-up Time Specification

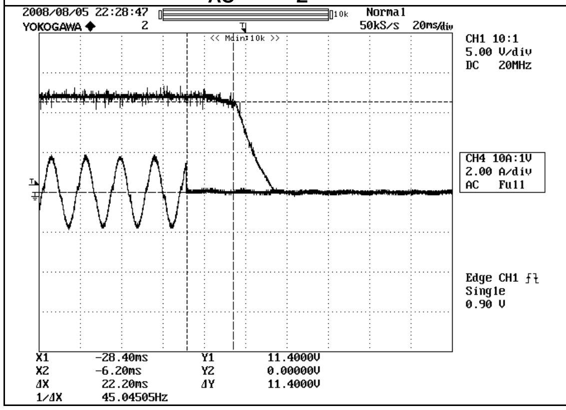
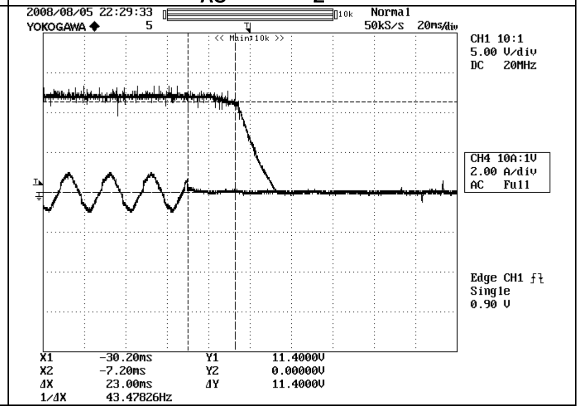
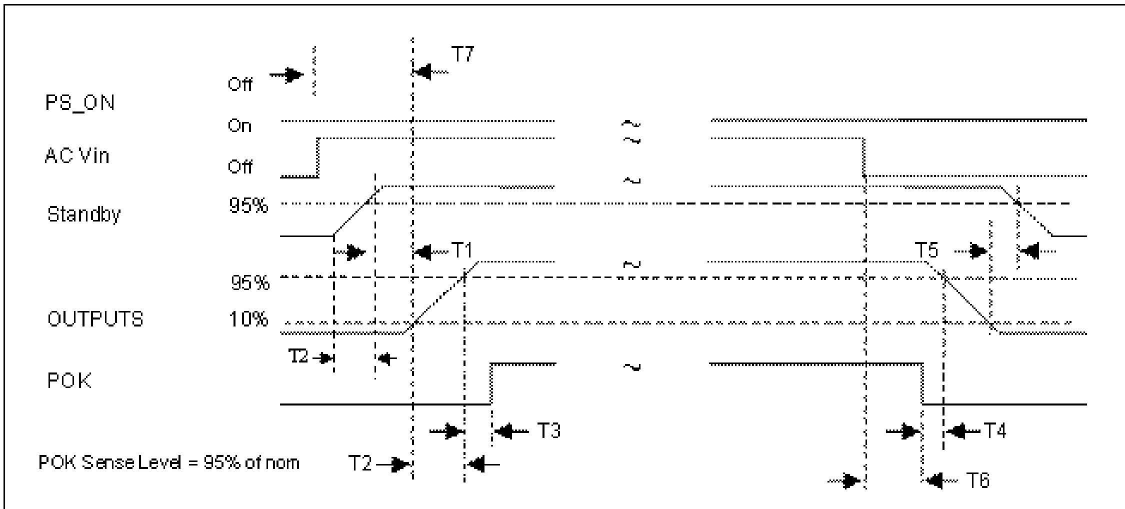
115 V_{AC} 60H_Z - 50% Load	230 V_{AC} / 50 H_Z - 50% Load
	

Figure 7: Hold-up Time

4.10 Timing / Housekeeping / Control

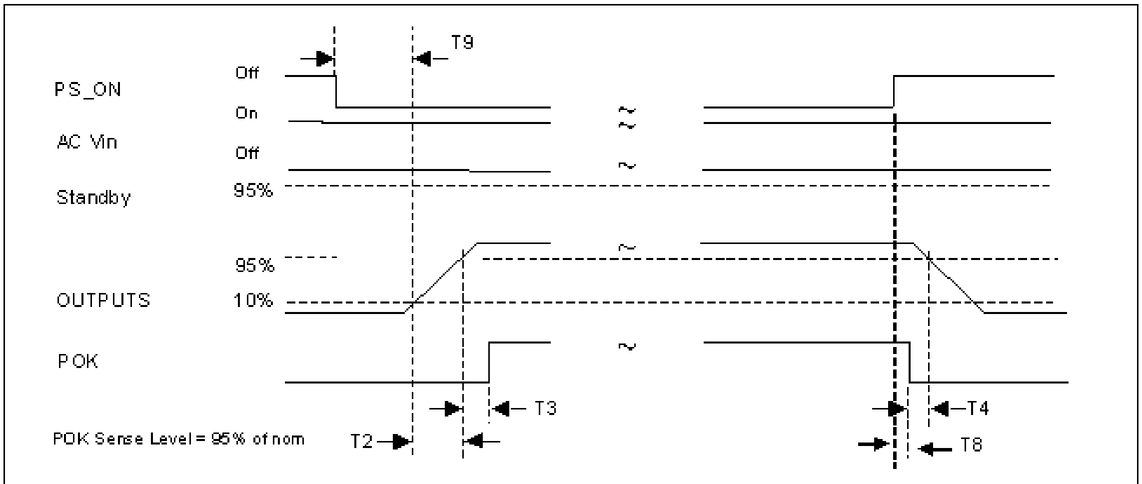
4.10.1 AC On / Off Control



AC On / Off Test	Parameter Description
Main Outputs Rise Time	2 ms < T2 < 20 ms
POK delay	100 ms < T3 < 500 ms
Power down warning	1 ms < T4
Hold-up time	T6 > 16 ms
PS_ON Timing (on)	T7 < 1000 ms
Main Outputs Rise Time	2 ms < T2 < 20 ms

Figure 8: AC On / Off Control

4.10.2 PS_ON On / Off Control



PS_ON On / Off Test	Parameter Description
Rise Time	2 ms < T2 < 20 ms
POK delay	100 ms < T3 < 500 ms
Power down warning	1 ms < T4
PS_ON Timing (off)	T8 < 60 ms
PS_ON Timing (on)	T9 < 350 ms
-12V_{DC} Rise Time	0.1 ms < T10 < 20 ms

Figure 9: PS_ON On / Off Control

4.10.3 Logic Timings

Parameter Description	Description	Min.	Max.	DC Output	Measurements		Units
					AC IN	PS_ON	
T1	Delay from Standby within regulation to DC outputs turn on	5	300	N/A	148	N/A	
T2	Standby, +3.3V_{DC}, +5V_{DC},and 12V_{DC} output rise time	2	20	+12V	2.8	4.2	
				+5V	2.6	2.4	
				+3.3V	2.8	2.2	
				+5Vsb	14	N/A	
T3	Delay from output voltages within regulation limits to POK asserted at turn on	100	500	+12V	250	256	
				+5V	244	250	
				+3.3V	244	252	
T4	Delay from POK deasserted to output voltages (3.3V, 5V, 12V, -12V) dropping out of regulation limits	1		+12V	1.6	28.4	
				+5V	4.8	30	
				+3.3V	6.8	32.4	
				-12V	6	12	
T5	Delay from DC output deasserted to Standby out of regulation at turn off.	5		+12V	608		ms
				+5V	600		
				+3.3V	600		
T6	Delay from loss of AC to desertions of PWOK.	16		N/A	604		
T7	PS_ON Timing (on)		1000	+12V	143		
				+5V	178		
				+3.3V	179		
T8	PS_ON Timing (off)		60	+12V		65.6	
				+5V		67.2	
				+3.3V		69.2	
T9	Delay from PS-ON reasserted to output turn on		350	+12V		80.8	
				+5V		86.8	
				+3.3V		86.8	
T10	-12V_{DC} output rise time	0.1	20	-12V	1.822	1.239	

Table 14: Logic Timings

4.10.4 PWR_OK

PWR_OK Full Load	CONTROL AND LOGIC SIGNALS RIPPLE/NOISE		
	Measurement	**Max.**	**Unit**
	35	400	mV_{P-P}

Table 15: PWR_OK Timings

4.10.5 PS_ON

PS_ON Full Load	CONTROL AND LOGIC SIGNALS RIPPLE/NOISE		
	Measurement	**Max.**	**Unit**
	30	400	mV_{P-P}

Table 16: PS_ON Timings

4.11 Output Protection

4.11.1 Output Over-Voltage Protection

DC Output	Specification		Measurements (V)
	Min. (V)	**Max. (V)**	
+12 $V_{A/B}$	13.5	15	
+5 V	5.6	7	6.36
+3.3 V	3.76	4.3	4.2
-12 V	-13.5	-15	
+5 V_{SB}	5.6	7	

Table 17: Output Over-Voltage Protection

4.11.2 Output Under-Voltage Protection

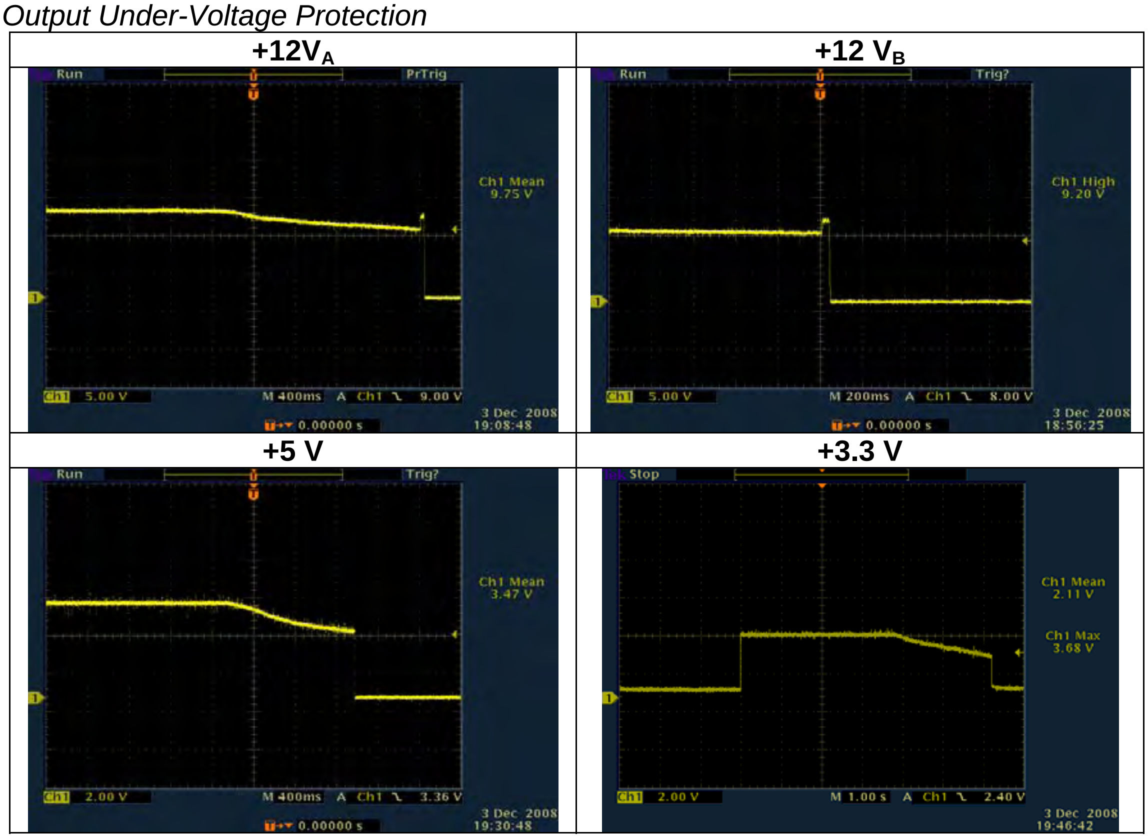
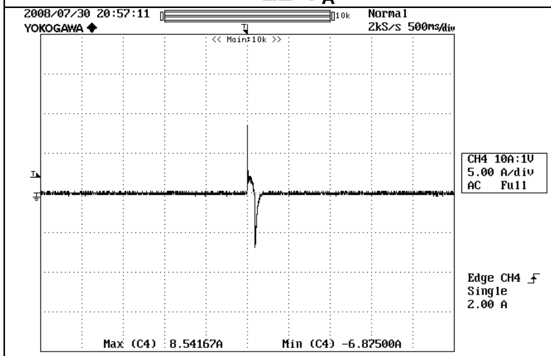


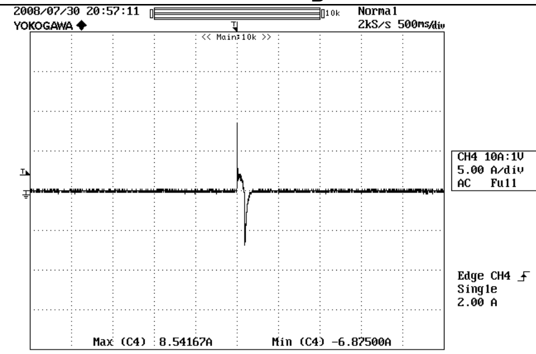
Figure 10: 115 V_{AC} / 60 H_Z DC Output Under-Voltage Protection @ Full Load

4.11.3 Short Circuit Protection

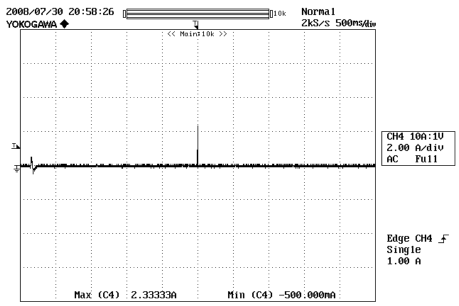
+12 V_A



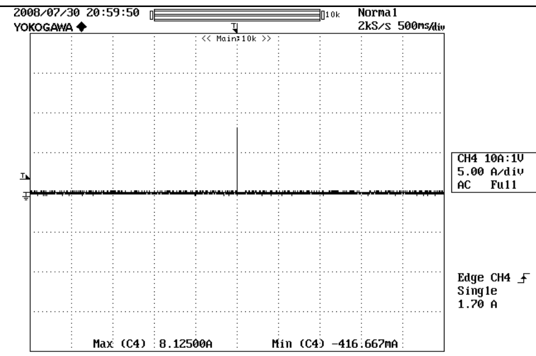
+12 V_B



+5 V



+3.3 V



+5 V_{SB}

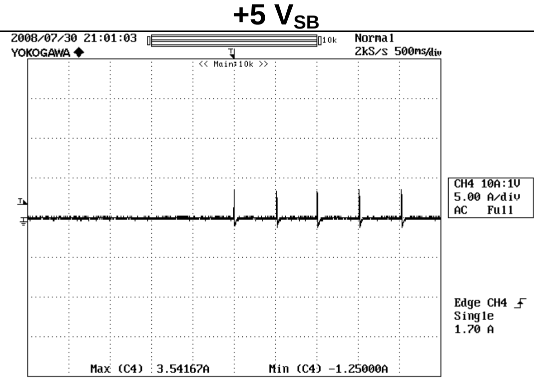


Figure 11: 115 V_{AC} / 60 H_Z DC Output Short circuit protection @ Full Load

4.11.3 Over-Current Protection

DC Output	Over Current Protection		Measurements (A)
	Min. (A)	Max. (A)	
+12 V_A	15	21 (< 240 V_{AC})	19.6
+12 V_B	8.5	11.5 (< 240 V_{AC})	10.0
+5 V	18	24	20.5
+3.3 V	10	13	10.9
-12 V	N/A	N/A	N/A
+5 V_{SB}	3	6	6.0

Table 18: Over-Current Protection

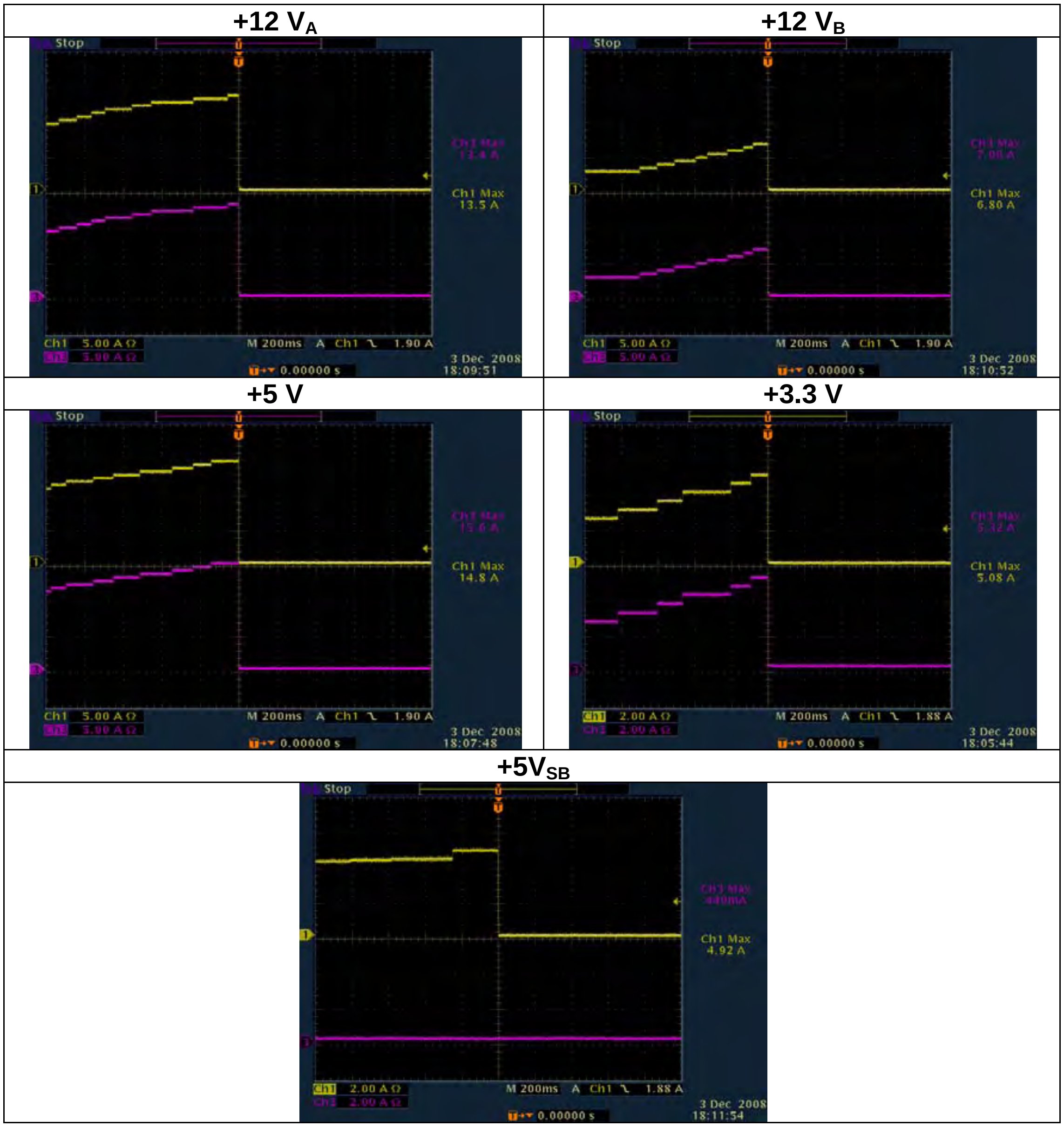


Figure 12: DC Output Short circuit protection @ Full Load

5. Evaluation Guidelines

Evaluation of the reference design should be attempted only by persons who are intimately familiar with power conversion circuitry. Lethal mains referenced voltages and high dc voltages are present within the primary section of the ATX circuitry. All testing should be done using a mains high-isolation transformer to power the demonstration unit so that appropriate test equipment probing will not affect or potentially damage the test equipment or the ATX circuitry. The evaluation engineer should also avoid connecting the ground terminal of oscilloscope probes or other test probes to floating or switching nodes (e.g. the source of the active clamp MOSFET). It is not recommended to touch heat sinks, on which primary active components are mounted, to avoid the possibility of receiving RF burns or shocks. High impedance, low capacitance test probes should be used where appropriate for minimal interaction with the circuits under investigation.

As with all sensitive switchmode circuitry, the power supply under test should be switched off from the ac mains whenever the test probes are connected and/or disconnected.

The evaluating engineer should also be aware of the idiosyncrasies of constant current type electronic loads when powering up the ATX demonstration unit. If the loads are adjusted to be close to the ATX's maximum rated output power, the unit could shut down at turn on due to the instantaneous overloading effect of the constant current loads. As a consequence, electronic loads should be set to constant resistance mode or rheostats should be used for loads. The other alternative is to start the supply at light to medium load and then increase the constant current electronic loads to the desired level.

The board is designed to fit in a traditional ATX enclosure as shown in Figure .

Figure 13: ON Semiconductor’s 255 W Reference Design for ATX Power Supplies

6. Schematics

The power supply is implemented using a single sided PCB board. Added flexibility is provided by using daughter cards for the PFC (NCP1654) circuit and the NCP1396 resonant mode controller. The individual PCB board schematics are shown in figure 14.

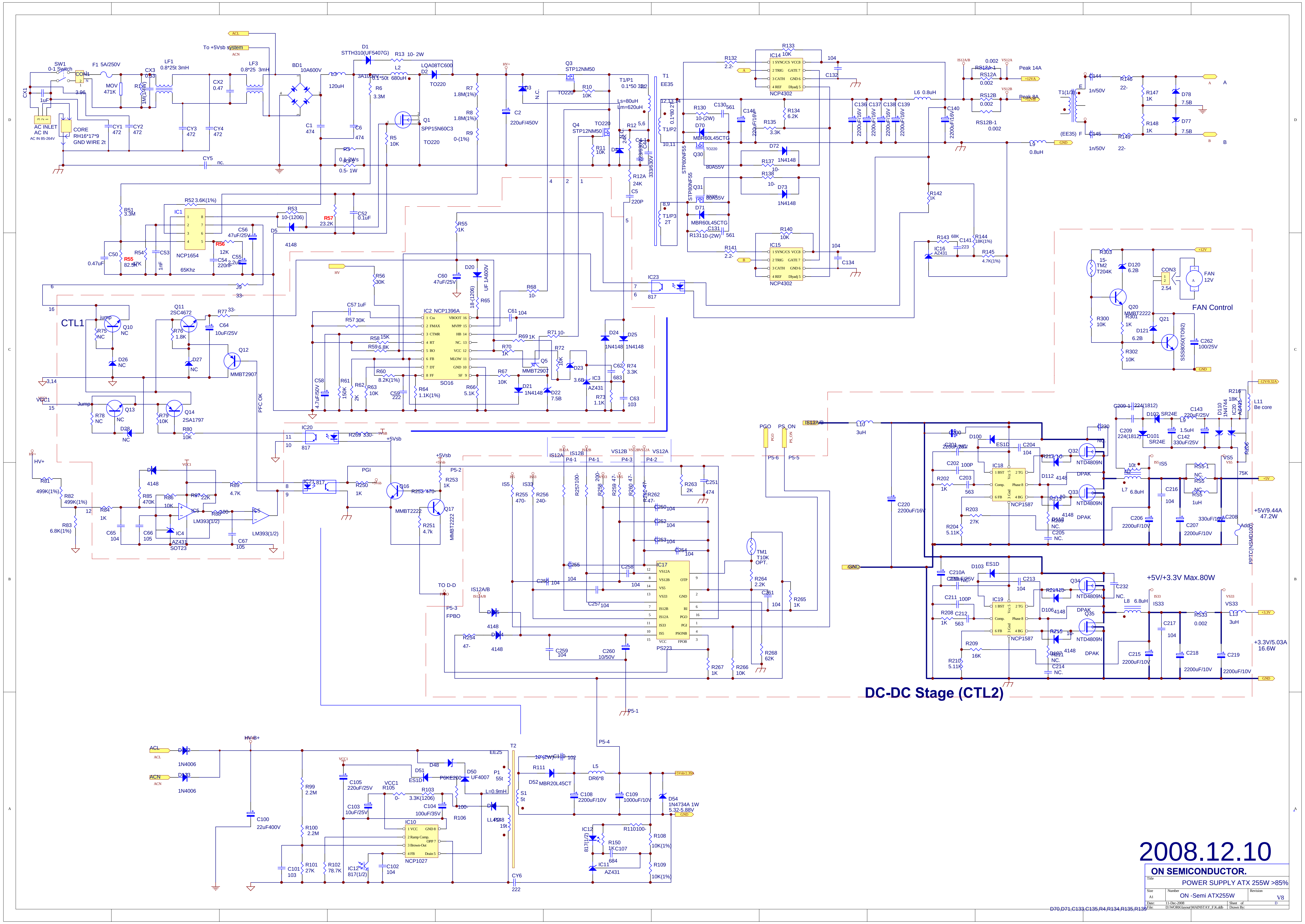


Figure 14: Schematics

7. Parts List

The bill of materials (BOM) for the design is provided in this section. To reflect the schematics shown in the previous section, the BOM have also been broken into different sections and provided in separate tables – Table 19 through 22.

It should be noted that a number of components used during the development cycle were based on availability. As a result, further cost reductions and better inventory management can be achieved by component standardization, i.e. the unique part numbers can be SIGNIFICANTLY reduced by standardization and re-use of component values and case sizes. This will result in a lower cost BOM and better inventory management.

QTY	SYMBOL	DESCRIPTION	VENDOR	VENDOR P/N
MAIN BOARD (PFC Stage, Synchronous Rectification Output Stage)				
1	HS1	HEAT SINK 93*60*4 AL4.0t	Taizhi	
1	BD1	DIO.BRI 10A 600V / TS10P05G	PANJIT	
1	D2	DIO.NR LQA08TC600 8A 600V TO-220AC	QSPEED	
1	Q1	FET.NCH SPP15N60C3 TO220	INFINEON	
2	Q3, Q4	FET.NCH STP12NM50 TO-220	ST	
1	SCREW(BD1)	SCREW PAN-HEAD M3*10	LONGFEI	
4	SCREW(D2, Q1, Q3, Q4)	SCREW PAN-HEAD M3*6	LONGFEI	
4	SL(D2, Q1, Q3, Q4)	SLTO-220 13*19*0.3mm	JUNHO	
4	B(D2, Q1, Q3, Q4)	BUSHING TO-220	JUNHO	
1	HS2	HEAT SINK 93*60*4 AL4.0t	Taizhi	
2	Q30, Q31	STP80NF55-06 80A55V TO220	ST	
1	D52,	MBR20L45CT 20A 45V TO-220	ON	
2	D70, D71	MBR60L45CTG 60A 45V TO-220	ON	
5	SCREW(D52, Q32, Q31, Q70, Q71)	SCREW PAN-HEAD M3*6	LONGFEI	
5	SL(Q30, Q31, D70, D71, D52)	SLTO-220 13*19*0.3mm	JUNHO	
5	B(Q30, Q31, D70, D71, D52)	BUSHING TO-220	JUNHO	
1	R3	RES.WW. 0.1R 3WS NKNP	Synton-Tech	
1	R13	RES.MO. 10- 2W	Synton-Tech	
3	R130, R131, R111	RES.CR. 10- 2WS	Synton-Tech	
1	D48	P6KE200A DO-15	PANJIT	
1	D50	UF4007 DO-41	PANJIT	
1	D1	STTH310 3A 1000V / UF5407G	DII	
1	C109	CAP.ELE 1000uF 10V 10*16KY	SU'SCON	
1	R1	RES.CR. 1M 1/4W		
3	RS12A, RS12A-1, RS12B	COPPER 0.002-		
1	F1	MST 5A/250V	CONQUER	
2	LF1.LF3	0.8*25t L=3mH+30% L=2.5mm	MEIHUA	(ASC-2203V-GH)25T
1	L2	POT3319 0.1Φ*50t*61t L=0.68uH	MEIHUA	
1	L3	T80-26+UL L=120uH±20%	MEIHUA	
1	L5	DR6*8 L=3.6uH	MEIHUA	
2	L6, L9	R8*20+UL L=0.8uH 2.4Φ*5.5t	J.X.E.	J-YH-R8*20-789

1	T1	YC3501 L=0.63mH Ls=80uH	MEIHUA	
1	T2	EE25	MEIHUA	
1	MOV	TVR10471KSY	TKS	
1	IC10	NCP1027P065G DIP-8	ON	
4	IC23, IC12, IC20, IC21	PHOTO PC817B DIP-4P	SHARP	
1	D54	1N4734A 1W 5.32-5.88V		
2	D122, D123	1N4006		
1	C4-1	CAP.PEI 0.022uF 630V		
1	C4	CAP.PEI 0.033uF 630V	PAC	R75PI2330JEMEJ
2	C1, C6	CAP.MEF 0.47uF 400V P=10	UTX	
1	CX3	CAP.MPP 0.33uF 275vac p=15	UTX	
1	CX2	CAP.MPP 0.47uf 275V HQX P=15	UTX	
1	C100	CAP.ELE 22uF 450V 8*11	SU'SCON	
1	C55	CAP.ELE 2.2uF 50V 5*11		
1	C2	CAP.ELE 220uf 450V	NDB	
1	C56	CAP.ELE 47uF 25V 5*11	NDB	
1	C105	CAP.ELE 220uF 25V 6.3*11	NDB	
1	C103	CAP.ELE 10uF 50V 5*11	NDB	
1	C104	CAP.ELE 100uF 35V 6*11	NDB	
5	C136, C137, C138, C139, C140	CAP.ELE 2200uF 16V 10*25 KZE	NDB	
1	C108	CAP.ELE 2200uF 10V 10*16	NDB	
1	C110	CAP.CER 1000PF 1KV Y5P P=5	SEC	2Y5P102K102C56E
2	C130, C131	CAP.CER 560PF 1KV Y5P	SEC	
1	C146	CAP.ELE 220uF 16V 6.3*11		
2	CY3, CY4	CAP.CER 4700PF Y2	SEC	
1	CY6	CAP.CER 2200PF Y1	SEC	
3	J4, J5, J6	JUMP 0.8Φ P=12.5mm		
3	J7, J19, J22	JUMP 0.8Φ P=20mm		
8	J1, J2, J3, J8, J11, J15, J18, J24	JUMP 0.8Φ P=10mm		
1	J23	JUMP 0.8Φ P=5mm		
1	MB CONNECT	MB CONNECT 24-PORT	EVERBIZ	
1	CPU CONNECT	CPU CONNECT 4-PORT(2*2)	EVERBIZ	
3	P3, P4, P5	SATA+SATA CONNECT	EVERBIZ	
2	P6, P7	SATA CONNECT	EVERBIZ	
2	P8, P9	FDD CONNECT 4-PORT	EVERBIZ	
2	HS3, HS4	HEAT SINK 28*38*5 CU1.2t	Taizhi	
1	CON1	WAFER 3.96(3-1)PIN 180°	SUNDA	
8	J10, J12, J13, J14, J16, R9, J20, R105	RES.SMD 0- 5% 0805		
1	J9	RES.SMD 33- 5% 0805		
1	J21	RES.SMD 0- 5% 1206		
1	R3-1	RES.SMD 0.5- 1% 2512		
5	R5, R10, R11, R133, R140	RES.SMD 10K 5% 0805		
2	R7, R8	RES.SMD 1.8M 5% 0805		
2	R12, R12A	RES.SMD 24K 5% 0805		

1	R54	RES.SMD 47K 1% 0805		
1	R55	RES.SMD 82.5K 1% 0805		
1	R56	RES.SMD 12K 5% 0805		
1	R57	RES.SMD 23.2K 5% 0805		
2	R51, R6	RES.SMD 3.3M 5% 0805		
1	R52	RES.SMD 3.6K 1% 0805		
2	R81, R82	RES.SMD 499K 1% 0805		
1	R83	RES.SMD 6.8K 1% 0805		
2	R99, R100	RES.SMD 2.2M 5% 0805		
1	R101	RES.SMD 27K 5% 0805		
1	R102	RES.SMD 78.7K 1% 0805		
1	R103	RES.SMD 3.3K 5% 1206		
6	R142, R147, R148, R250, R253, R150	RES.SMD 1K 5% 0805		
2	R108, R109	RES.SMD 10K 1% 0805		
1	R110	RES.SMD 100- 5% 0805		
2	R132, R141	RES.SMD 2.2- 5% 0805		
1	R134	RES.SMD 6.2K 5% 0805		
1	R135	RES.SMD 3.3K 5% 0805		
2	R137, R138	RES.SMD 10- 5% 0805		
1	R53	RES.SMD 10- 5% 1206		
1	R143	RES.SMD 68K 5% 0805		
1	R144	RES.SMD 18K 1% 0805		
1	R145	RES.SMD 4.7K 1% 0805		
2	R146, R149	RES.SMD 22- 5% 0805		
1	R251	RES.SMD 4.7K 5% 0805		
1	R252	RES.SMD 470- 5% 0805		
1	R269	RES.SMD 330- 5% 0805		
1	C5	CAP.MON 220P 50V 0805 X7R		
1	C50	CAP.MON 0.47uF 50V X7R 0805		
2	C101, C102	CAP.MON 0.01uF 50V X7R 0805		
2	C107, C54	CAP.MON 0.22uF 50V X7R 0805		
3	C53, C144, C145	CAP.MON 1000PF 50V X7R 0805		
3	C134, C132, C52	CAP.MON 0.1uF 50V X7R 0805		
1	C141	CAP.MON 0.022uF 50V X7R 0805		
1	D51	ES1D 1A 200V SMA	TSC	
4	D5, D72, D73, D49	DIO.NR LL4148	TSC	
2	D77, D78	DIO.ZEN RLZ7.5B	ROHM	
2	Q16, Q17	MMBT2222 SOT23		
1	IC1	NCP1654A 65Khz SO-8	ON	
2	IC11, IC16	TL431	ON	
2	IC14, IC15	NCP4302 SO-8	ON	
1	PCB	CEM-1 1oz 1.6t 145*108.5 NO.SPB011V5		

Table 19: Main Board (PFC Stage, Synchronous Rectification Output Stage)

QTY	SYMBOL	DESCRIPTION	VENDOR	VENDOR P/N
DC-DC Converter Stage, Supervisory Stage (referred to as CTL2 in schematics of figure 14)				
1	C220	CAP.ELE 2200uF 16V 10*25	NDB	
1	L11	BEAD RH035100ST-A8		
1	RS33	COPPER 0.002-	Tzai Yuan	
1	C208	CAP.ELE PSC 680uF 10V 10*11.5	NDB	
5	C206, C207, C215, C218, C219	CAP.ELE 2200uF 16V 10*25	NDB	
1	C260	CAP.ELE 10uF 50V 5*11 KY	NDB	
1	C142	CAP.ELE 330uF 25V 8*15 KY	NDB	
1	C143, C200, C200A	CAP.ELE 220uF 25V KY 6.3*11	NDB	
1	C209	CAP.PEI 0.47uF 100V P=10	欣統	
1	C262	CAP.ELE 100uF 25V 6.3*11	NDB	
1	D110	1N4744		
1	Q21	S8050L-C EBC TO92	UTC	
1	L7	HKH080 L=6.8uH		
1	L8	HKH080 L=6.8uH	MEIHUA	HKH-080CE/034
1	L9	DR6*8 L=3.6uH	MEIHUA	
2	L10, L13	R6*20+UL L=3.0uH±20% 1.2Φ*11.5t	MEIHUA	R6*20-0003
1	RS5	R8*20+UL L=1uH±20%		
1	TM1	T10K	TKS	TTC05103KSY
1	TM2	T204K	TKS	TTC05204KSY
1	HS7	HEAT SINK 25.5*12.5 Cu1.2t	Taizhi	
2	HS8, HS9	HEAT SINK 40.5*12.5 Cu1.2t	Taizhi	
1	CON3	WAFER P=2.5*2 90°	SUNDA	
1	P4(CTL3-PCB)	Pin Header 3pin 90° P=2.54mm	SUNDA	
1	P5(CTL3-PCB)	Pin Header 6pin 90° P=2.54mm	SUNDA	
1	PPTC	Fuse 1A 1206	CONQUER	nSMD100
3	R266, R300, R302	RES.SMD 10K 5% 0805		
1	R203	RES.SMD 27K 1% 0805		
2	R204, R210	RES.SMD 5.11K 1% 0805		
4	R212, R214, R213, R215	RES.SMD 10- 5% 0805		
1	R206	RES.SMD 75K 5% 1206		
1	R216	RES.SMD 18K 5% 1206		
1	R209	RES.SMD 16K 1% 0805		
5	R254, R259, R260, R261, R262	RES.SMD 47- 5% 0805		
1	R255	RES.SMD 470- 1% 0805		
1	R256	RES.SMD 240- 1% 0805		
1	R257	RES.SMD 100- 1% 0805		
1	R258	RES.SMD 200- 1% 0805		
1	R263	RES.SMD 2K 5% 0805		
1	R264	RES.SMD 2.2K 5% 0805		
5	R265, R267, R301, R202, R208	RES.SMD 1K 5% 0805		
1	R268	RES.SMD 62K 1% 0805		
1	R303	RES.SMD 15- 5% 0805		
2	C209, C209-1	CAP.MON 0.22uF 50V X7R 1812		
14	C204, C213, C216, C217, C250, C252, C253, C254, C255, C256, C257, C258, C259, C261	CAP.MON 0.1uF 50V X7R 0805		
2	C202, C211	CAP.MON 100P 50V X7R 0805		
2	C203, C212	CAP.MON 0.056uF 50V X7R 0805		

1	C251	CAP.MON 0.47uF 16V X7R 0805		
2	D100, D103	ES1D 1A 200V SMA	TSC	
2	D101, D102	DIO.SB SR24 2A 40V SMA	PANJIT	
6	D104, D105, D112, D113, D106, D107	DIO.ZEN LL4148	TSC	
2	D120, D121	DIO.ZEN RLZ6.2B	ROHM	
1	Q20	MMBT2222 SOT23		
4	Q32, Q33, Q34, Q35	NTD4809N-D 58A 30V DPAK	ON	
1	IC17	PS223 SOP-16	SITI	
2	IC18, IC19	NCP1587 SO-8	ON	
1	IC20	TL431	ON	
1	PCB	FR4 1oz 1.6t 62*83.5 NO.PB011V5-CTL3		

Table 20: DC-DC Converter Stage, Supervisory Stage (referred to as CTL2 in schematics of figure 14)

P/N	QTY	SYMBOL	DESCRIPTION	VENDOR	VENDOR P/N
HB Resonant LLC-Stage (referred to as CTL1 in schematics of figure 14)					
	1	C58	CAP.ELE 4.7uF 50V KMG 5*11	NDB	
	1	C60	CAP.ELE 47/25V KMG 5*11	NDB	
	1	C64	CAP.ELE. 10uF 25V	NDB	
	1	P2 (CTL2-PCB)	Pin Header 3pin 90° P=2.54mm	SUNDA	
	1	P3 (CTL2-PCB)	Pin Header 13pin 90° P=2.54mm	SUNDA	
	1	HS	25*16*8		
	1	PCB HOLD	RCC-5	KANGYANG	
	4	R55, R69, R70, R84	RES.SMD 1K 5% 0805		
	2	R56, R57	RES.SMD 30K 5% 0805		
	1	R58	RES.SMD 15K 5% 0805		
	1	R59	RES.SMD 6.8K 5% 0805		
	1	R60	RES.SMD 8.2K 1% 0805		
	1	R61	RES.SMD 150K 5% 0805		
	1	R62	RES.SMD 2K 5% 0805		
	2	R64, R73	RES.SMD 1.1K 1% 0805		
	6	R63, R67, R72, R79, R80, R86	RES.SMD 10K 5% 0805		
	1	R65	RES.SMD 18- 5% 1206		
	1	R66	RES.SMD 5.1K 5% 0805		
	2	R68, R71	RES.SMD 10- 5% 0805		
	1	R74	RES.SMD 3.3K 5% 0805		
	1	R76	RES.SMD 1.8K 5% 0805		
	1	R77	RES.SMD 33- 5% 0805		
	1	R88	RES.SMD 100- 5% 0805		
	1	R85	RES.SMD 470K 5% 0805		
	1	R87	RES.SMD 22K 5% 0805		
	1	R89	RES.SMD 4.7K 5% 0805		
	1	C59	CAP.MON 2200PF 50V X7R 0805		
	2	C61, C65	CAP.MON 0.1uF 50V X7R 0805		
	1	C62	CAP.MON 0.068uF 50V X7R 0805		
	1	C63	CAP.MON 0.01uF 50V X7R 0805		
	3	C66, C67, C57	CAP.MON 1uF 25V X7R 0805		
	1	D20	UF 1A600V / US1J	PANJIT	
	4	D21, D24, D25, D29	DIO.ZEN. LL4148	TSC	
	1	D22	DIO.ZEN. RLZ7.5B	ROHM	
	1	D23	DIO.ZEN. RLZ3.6B	ROHM	
	2	Q5, Q12	MMBT2907	PANJIT	
	1	Q11	2SC4672	ROHM	
	1	Q14	2SA1797	ROHM	
	1	IC2	NCP1396A SO-16	ON	
	2	IC3, IC4	TL431	ON	
	1	IC5	LM393 SO-8	ON	LM393D
	1	PCB	FR4 1oz 1.6t 44*56 NO.SPB011V4-CTL2		

Table 21: HB Resonant LLC-Stage (referred to as CTL1 in schematics of figure 14)

QTY	SYMBOL	DESCRIPTION	VENDOR	VENDOR P/N
Mechanical and Miscellaneous Items				
1	SW1	0-1 4P 10A Look SW	SWEETA	SS21-BBIWG-R
1	SW-INLET	UL1015#18 L=115mm	CHARNG MIN	
1	SW-INLET	UL1015#16 L=60mm White	CHARNG MIN	
1	SW-INLET	UL1015#16 L=60mm Black	CHARNG MIN	
1	INLET(G)-GND	UL1015#18 L=125mm	CHARNG MIN	
1	CORE(INLET-GND)	RH16*9*17		
1	DTOD-BOARD			
1	FAN	80*80*25mm 12V	SUNON	
2	CY1, CY2	CAP.CER 4700PF Y2	SEC	
1	CX1	CAP.MPP 1uF 275VAC HQX P=22.5	UTX	
1	AC INLET	10A/15A 250V	SWEETA	SC-9-1
1	CASE	CASE 150.2*140*84mm		
1	CASE	CASE 140*148.2*85.5mm		
1	MYLAR	MYLAR FILM 165*110*0.35mm	JUNHO	
2	SCREW(AC INLET)	SCREW F3*10 ISO(BLACK)	LONGFEI	
4	SCREW(CASE)	SCREW F3*6 ISO(BLACK)	LONGFEI	
1	SCREW(INLET-GND))	SCREW F3*5 ISO(BLACK)	LONGFEI	
4	SCREW(S1~S4)	SCREW MAIN BOARD M3*4 ISO	LONGFEI	
4	SCREW(FAN)	SCREW I5*10 TAP (BLACK)	LONGFEI	
1	SCREW(GND)	SCREW K/NUT 8#32T	LONGFEI	
1		FAN GUARD 80*80mm COLOR-GOLD	PRO-CROWN	
1		SANP BUSHING NB-27A	KANGYANG	

Table 22: Mechanical and Miscellaneous Items

8. Resources/Contact Information

Data sheets, applications information and samples for the ON Semiconductor components are available at www.onsemi.com. Links to the datasheets of the main components used in this design are included in the Appendix.

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9. Appendix

Link to ON Semiconductor's web site:

- ON Semiconductor Home Page

Industry information links:

- ENERGY STAR
- 80 PLUS Efficiency Requirements
- Climate Savers Computing Initiative
- IEC61000-3-2 Requirements
- ATX 12 V Form Factor
- European Union (EU) Energy Star Page

Additional collateral from ON Semiconductor:

- **NCP1654** Continuous conduction mode PFC controller
- **NCP1396** Resonant mode controller with high voltage drivers
- **NCP4302** Synchronous rectification controller
- **NCP1587** Low voltage synchronous buck controller
- **NCP1027** High voltage integrated switcher
- **NTD4809** Single N-Channel MOSFET 30 V, 58 A
- **MBR20L45** 20 A, 45 V dual schottky rectifier

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